

## **Design, Implementation and Simulations of Digital Voting Machine Using Full Adders and Parallel Binary Adders**

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### *Abstract*

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*In this work, a digital voting machine was designed, implemented and simulated. The design was carried- out using 4- bit parallel binary adders (74LS283) and full adders. It is simple electronic voting system that can be used to simultaneously provide the number of "yes" votes and the number of "no" votes. It can be used where a group of people are assembled and there is a need for immediate determination of opinions (for or against), making decisions, or voting on certain issues or other matters. The system includes switches for "yes" or "no" selection at each position in the assembly and digital display for the number of "yes" votes and one for the number of "no" votes. The system was designed to accommodate total of twenty four members of the assembly with possible increase to higher number. It was implemented and simulated on national instrument software 'multisim' version 11.0. It was tested and found to be working as designed.*

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**Keywords:** tuberculosis, homotopy analysis method, nonlinear equations, mathematical model, epidemics

### **1.0 Introduction**

A voting system is a method by which voters often make a choice between options in an election or a policy referendum. It is a key factor for resolving issues in places like parliaments, company board of directors, group of law makers, national election etc. In most critical cases such as national elections, nominations, voting for or against an issue, the voter encounter much problem in casting his vote in the presence of contestants and need a way of casting his vote secretly. The problems of voting with ballot papers include the following.

- 1) Inability of a voter to change his decision after the vote is already casted.
- 2) Lack of privacy on the side of the voter because at least one of his identity such as thumbprint can be tracked and he can be victimized.
- 3) Using ballot paper in voting is time consuming because the votes has to be counted one after the other before the result is obtained.
- 4) Transparency is very low when voting with ballot papers, this is because the voter cannot see the result until all voters finished casting and the result is counted.
- 5) High cost of printing ballotpapers and other accessories make ballot voting expensive.
- 6) After voting, the ballot papers cannot be used for another voting exercise and that implies waste of resources.

Many related problems which are not listed may be encountered when voting manually with ballot papers. One way to solve the aforementioned problems is the use of a digital electronic voting machine.

There were several attempts to design a digital voting machine from simple circuit using discrete logic gates to one with complicated circuits using hardware description language (HDL) in programmable logic devices [1, 2]. Many use programmable integrated circuit (PIC) while few use discrete logic gates in their implementations.

Here we intend to discuss the design, implementation and simulation of digital voting machine using binary full adder and parallel binary adders. The system includes switches each of which has three positions, one position to vote for "YES" another position to vote for "NO" (which can be used to vote "FOR" or "AGAINST" an option) and the last position is for

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undecided vote which is not counted by the parallel adder. The system consist of twenty four switches one for each voter; which makes the system suitable for maximum of 24 voters, however it can be expanded to accomodate to any number of voters. The voting machine also include a counter with two seven segment display. One display the count for "YES" and the other display the count for "NO". The display can also be used to vote for two parties, one for each party.

In this work the voting machine is designed to minimize the problems of manual voting system. Hence, this machine can be used in a parliament where the voter need not to go closer to the device before casting his vote, rather he can cast his vote on his table by just pressing a button and the result is automatically displayed on a screen.

**1.1 Advantages Of Digital Voting Machine**

The benefits which can be derived from digital voting machine include the following.

- 1) A voter has the alternative of changing his decision even after the vote has already been casted by just switching to his choice when the voting is in progress.
- 2) Privacy is guaranteed when using digital voting machine because the voter can cast his vote by just pressing a button of his choice unidentified without leaving his position.
- 3) Time is effectively conserved because the votes are counted automatically and the result is displayed on the screen when the voting is in progress.
- 4) Using digital voting machine is highly transparent because the voter can see the results immediately he finished casting his vote.
- 5) Cost of implementation is low compare to that of ballot voting.
- 6) The problem of wastage of resources is solved because the voting machine can also be used in future voting exercises.
- 7)

**1.2 BINARY ADDERS**

An important function of digital systems and computers is the execution of arithmetic operations. A basic binary adder consists of half adder and a number of full adders depending on the number of bits of the binary words to be added. A half adder adds a bit from addend and another from augends at the least significant stage, generating a SUM output and a CARRY output. A full adder adds a carry from the less significant stage, a bit from addend and a bit from augends at present stage, generating a SUM and a CARRY outputs[3].

**1.2.1 Half-Adder**

The half-adder is a combinational circuit that generates the result of adding two 1-bit binary values. One output gives the *sum* bit, and the other gives the *carry* bit. This circuit is called a half-adder because it does not accept a carry bit as input, but it does generate an output carry bit. The truth table for a 1 bit two variable half-adder and the corresponding logic circuit is shown in Table 1 and Figure 1 respectively.

TABLE 1: Half adder truth table

A	B	Sum	carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

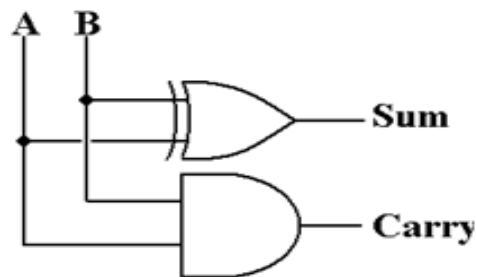


Figure 1. Logic symbol of half adder

**1.2.2 Full-Adder**

The full-adder has the same orientation as the half-adder except that it accepts a carry bit as input with the two input bits. Therefore, the full adder has three bits input and generates at the outputs a *sum* and a *carry* bit. The additional carry input bit will double the number of possible input bit patterns from four to eight[4]. The truth table and logic diagram of a full adder is shown in Table 2 and Figure 2 respectively.

TABLE 2: Truth Table of Full Adder

A	B	C <sub>in</sub>	SUM	C <sub>out</sub>
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

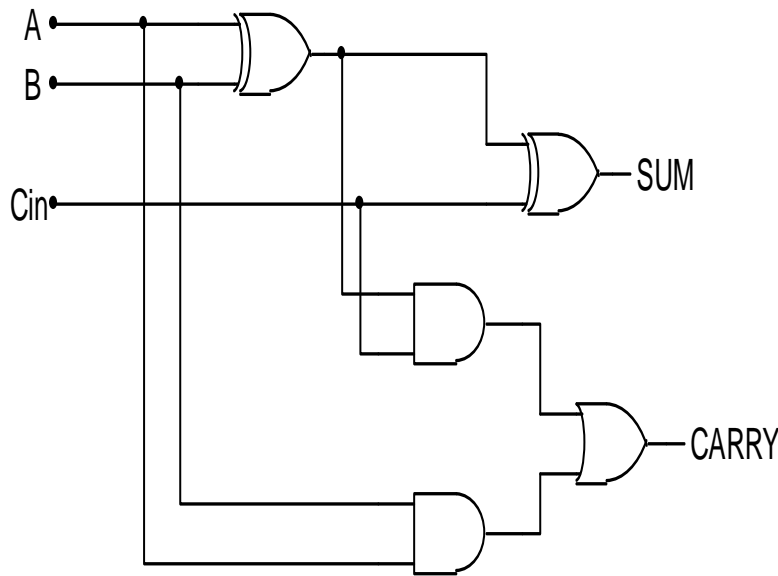


Figure 2: Logic symbol of full adder

The equations for the sum and carry of a full adder are as follows.

$$\Sigma(A,B,C) = (A \oplus B) \oplus C_{in} \tag{1}$$

$$C_{out} = (A \oplus B)C_{in} + AB \tag{2}$$

## 2.0 Methodology

The implementation of voting machine utilizes a four bit parallel adder and full adders. The four bit parallel adder consists of four full adder circuit cascaded through their input and output carries. The least significant bit (LSB A<sub>1</sub> & B<sub>1</sub>) in any group of numbers is being added to the rightmost bit of the next full adder. The higher-order bits are also applied to successive higher-order adder with the most significant bit (A<sub>4</sub> & B<sub>4</sub>) in each number applied to the leftmost full adder. The block diagram and the logic symbol of a four bit parallel adder is shown in Figure 3 and the truth table for the four bit parallel adder is shown in Table 3 [3, 4, 5].

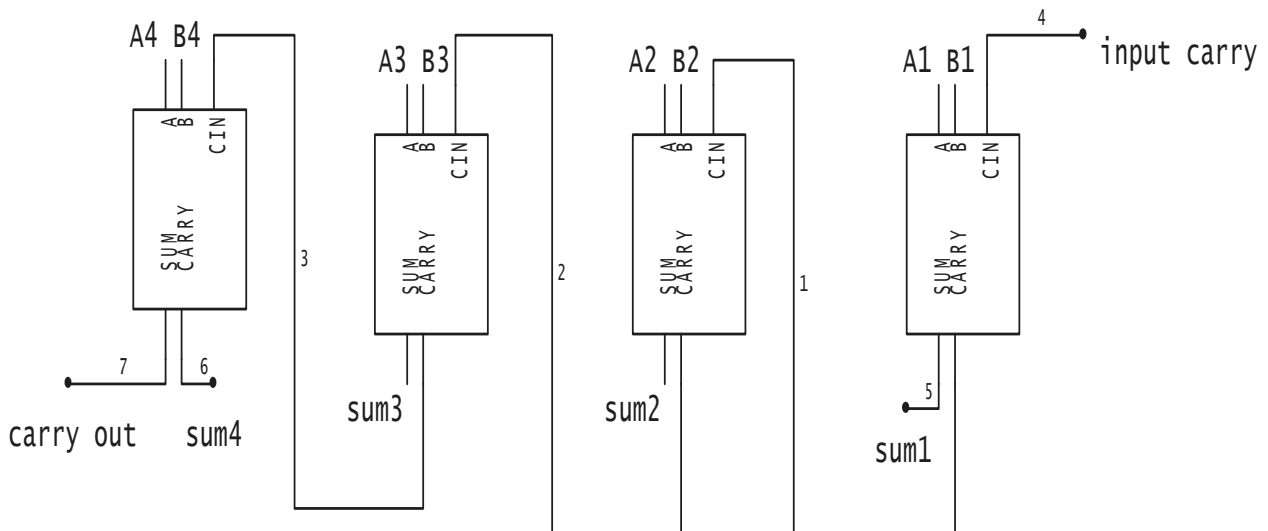


Figure 3: parallel addition of binary numbers.

TABLE 3: Truth table of a parallel

$C_{n-1}$	$A_n$	$B_n$	$\Sigma_n$	$C_n$
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Figure 4 shows the functional diagram and logic symbol for a 74HC283 parallel adder. From the figure, it can be seen that the least significant binary input  $2^0$  is passed through the  $A_1B_1$  terminals and the most significant  $2^3$  into the  $A_4B_4$  terminals. The carry-out ( $C_{out}$ ) from each full adder is internally connected to the carry-in ( $C_{in}$ ) of the next full adder. The carry-out of the last full adder is utilized as the sum  $\Sigma_5$  output making the 5<sup>th</sup> bit sum or to be used as a carry-in ( $C_{in}$ ) to the next full adder IC; if more than four bits are to be added. An important feature of the 74HC283 IC is the **fast look-ahead carry**. The fast look-ahead carry is very important for speeding up the arithmetic process. For example if we are adding two 8-bit numbers using the 74HC283 IC the fast look ahead carry evaluates the four lower-order inputs,  $A_1B_1$  to  $A_4B_4$  to determine if they are going to produce a carry-out out of the fourth full adder to be passed on the next higher-order adder IC [1,5,6]. In this way, the addition of the higher order bits ( $2^4$  to  $2^7$ ) can take place concurrently with the lower order ( $2^0$  to  $2^3$ ) addition without having to wait for the carries to propagate (or ripple) through  $FA_1$  to  $FA_4$  to become available to the higher order addition [5, 6, 7].

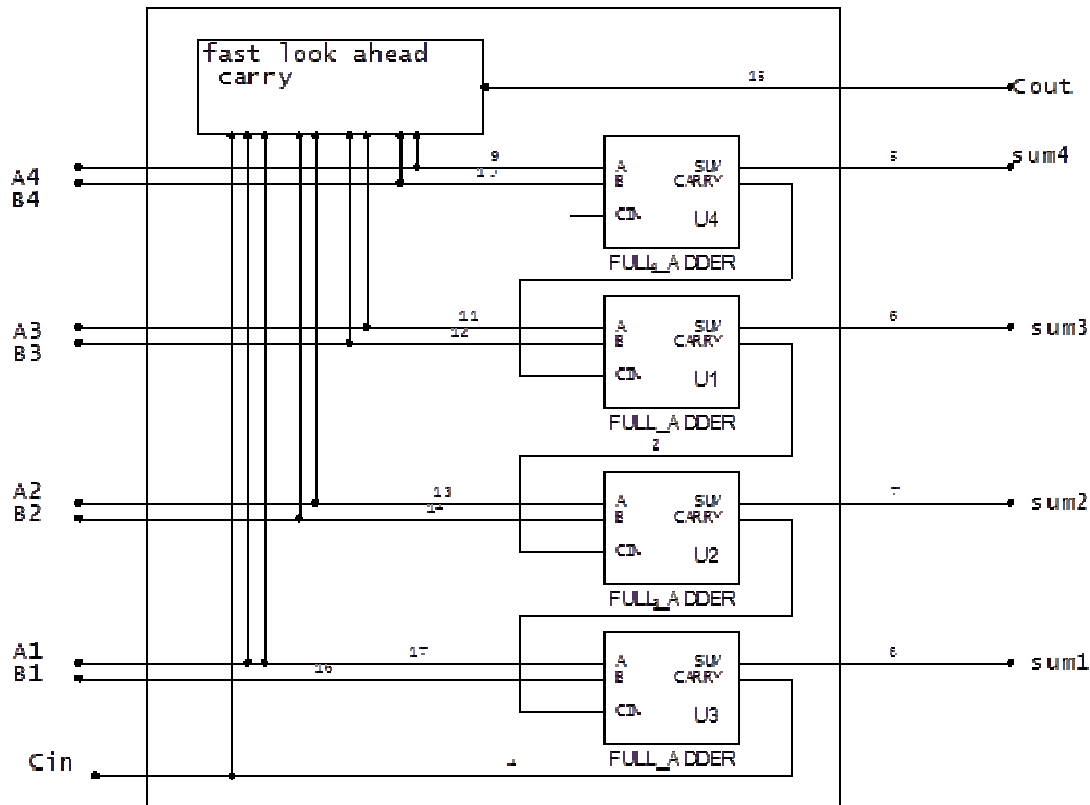


Figure 4: Internal configuration of a 74HC283 parallel adder.[5]

## 2.1 The Input Selection Section

The inputs consist of twenty four switches of three positions each, one position of the switch is set to vote for “YES”, the second position of the switch is set to vote for “NO”, and the last position for undecided vote. The two positions (the ‘yes’ and the ‘no’ positions) are counted by the parallel adder and the result is displayed at the output while the last position set for the undecided is not displayed. If any of the switches is toggled, a binary bit which can be either a 1 or a 0 is generated at the input of one of the full adder [7]. The three inputs of the full adder (that is the two inputs and the carry input) are summed up, a sum and a carry are generated at the output. The input of the machine is design in such a way that a voter may choose between two options each of which is counted by a particular adder as shown in Figure 5.

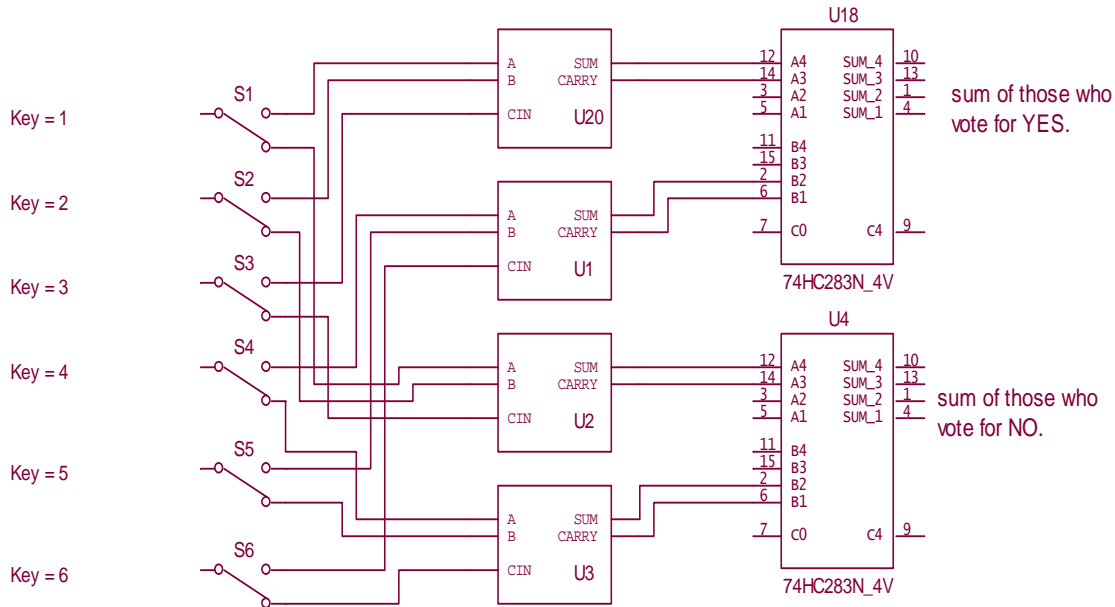


Figure 5: Input of the voting machine

A full adder can only sum up to three binary levels (01, 10 & 11). Therefore when two adders are used on the lower order input the parallel adder sum up the two outputs of the full adders and display the resulting sum as shown in Figure 6.

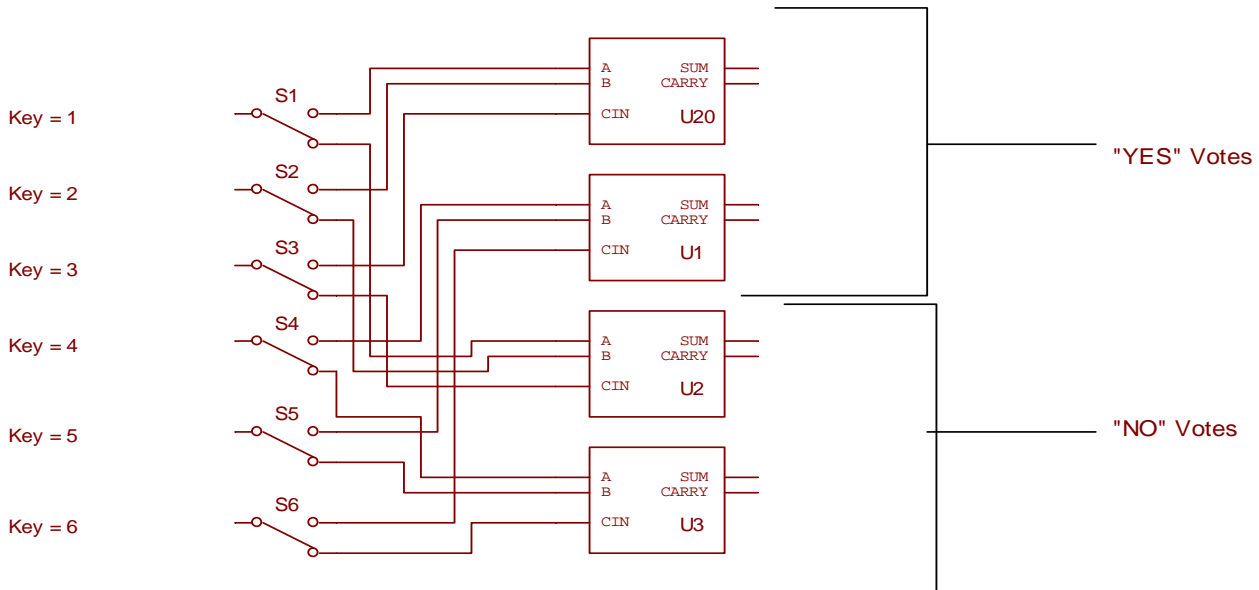
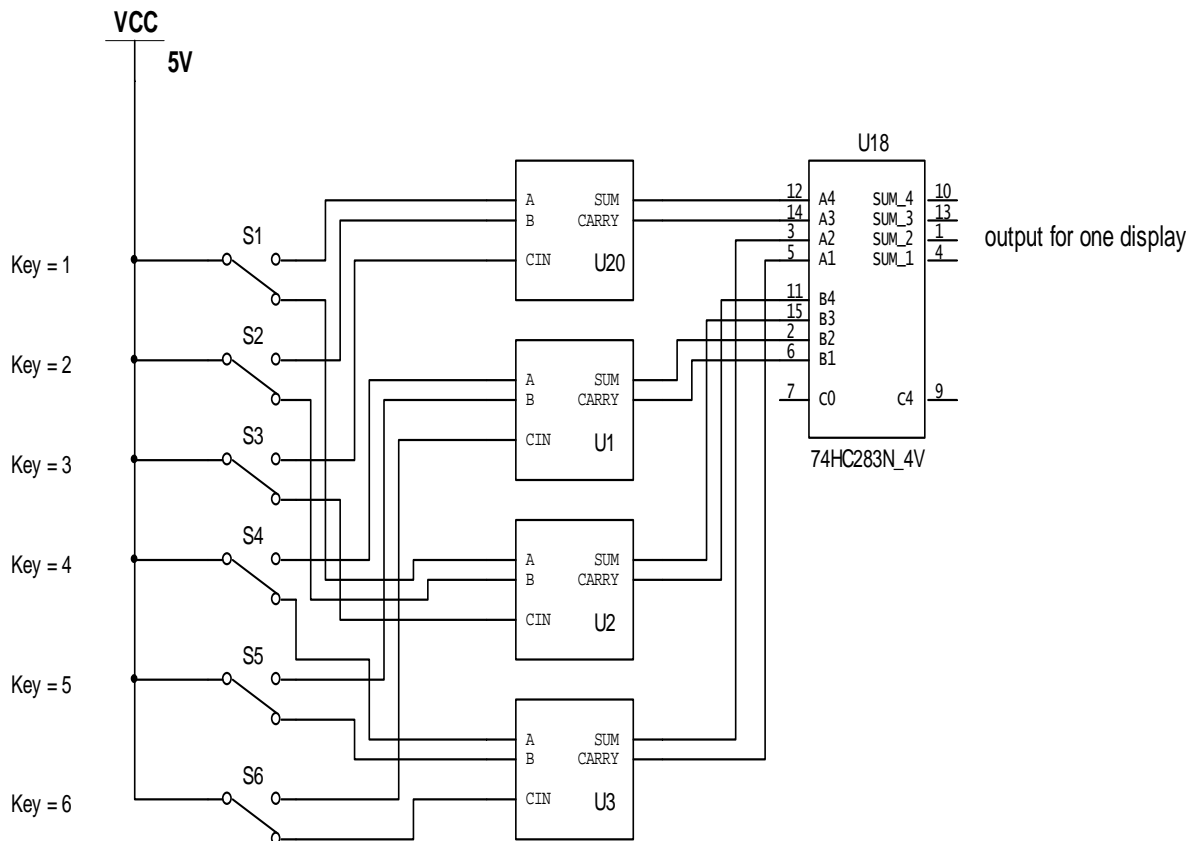


Figure 6: Cascading full adder with parallel adder



**Figure 7: Sum of all the inputs appear as a single output.**

One of the key advantage of using the parallel adder is that when the output of the two or more full adders are coupled to the remaining four higher-order inputs of the parallel adder, the parallel adder sum up all the inputs together (i.e.  $3 \times 4 = 12$  inputs). The whole of these setups can be taken as a single conditional input (i.e. the number of those who voted for YES). The same setup is also implemented for the voters who voted for NO using the same setup as described. However, the output of two parallel adders (IC part number 74213) serves as input for another separate parallel adder, which produces the sum of all the inputs applied to it so as to increase the number of voters. Hence, it can be used to increase the number of voters to any number needed with additional adder circuits. The logic diagram of the full adder connected to a display is shown in Figure 7.

The output of the full adder is fed into the input of the parallel adder and the sum of all the votes appear at the output of the parallel adder as a sum and a carry. The circuit can be expanded to any number of voters and contestants by the addition of the half adder connected to the input of a parallel adder and the inputs is either increased to suite the number of voters, or replaced by an additional circuitry which can accommodate large number of voters [6, 8]. The cascading of the parallel adder is shown Figure 8.

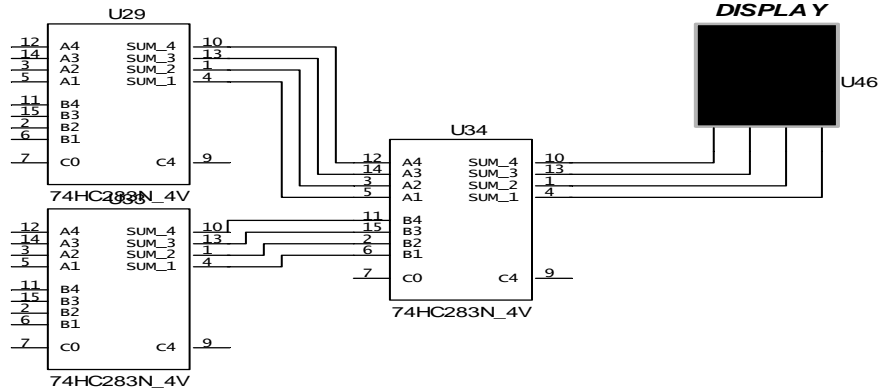


Figure 8: Cascading parallel adders.

### 2.2 The Outputdisplay

The output of the voting machine generates 5-bits binary number. When these binary numbers are fed directly to the display, the display displayed it in hexadecimal because the 5-bit numbers exceeded to the invalid Binary Coded Decimal (BCD) codes. Hexadecimal numbering is difficult to be interpreted by the observers and is not viewer friendly as shown in Figure 9.

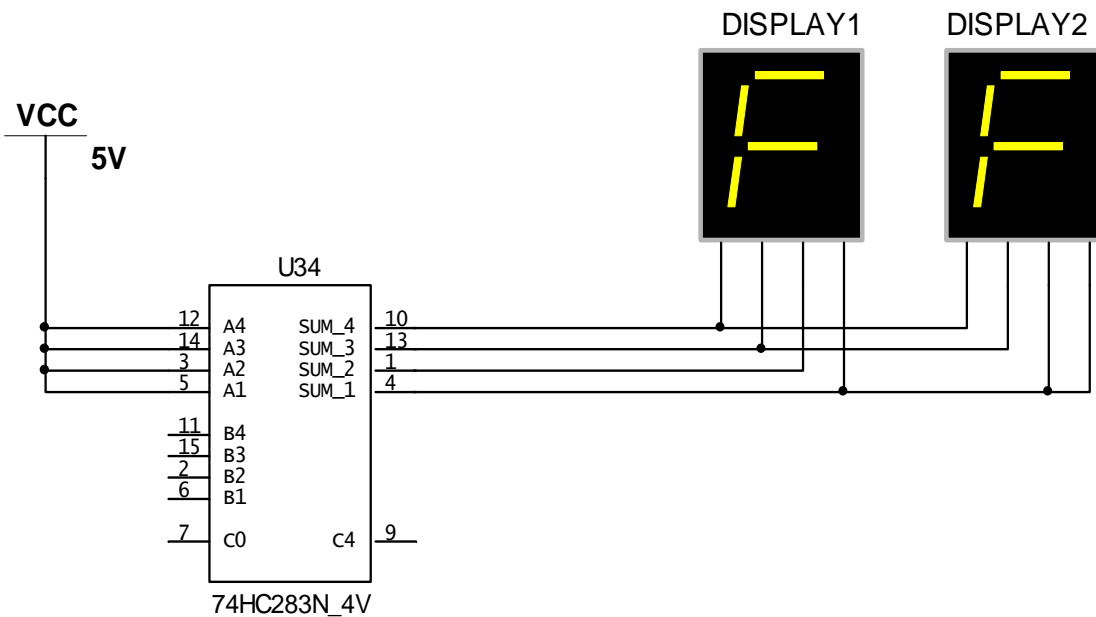


Figure 9: Output display.

Thus, for proper decimal display, additional circuitries are needed to convert the hexadecimal numbers to a form more suitable and acceptable by the users, which is the decimal numbers system. This converter detect the hexadecimal numbers from nine to sixteen (i.e. A,B,C,D,E&F) and add a binary numbersix (0110) to skip the invalid BCD state to a valid BCD state for proper display of the corresponding decimal equivalent.

### 2.3 Hexadecimal Conversion.

The hexadecimal converter is design by writing down the binary equivalent of the invalid BCD codes so that whenever the result to be displayed is between these numbers the detector will add six (0110) to the result to skip the invalid state. However, if a carry is also produce by the result making it a 5-bit digit the addition of six is also made. For the design karnaugh mapping is utilize by writing down the logic function of the hexadecimal numbers is as follows.



$$F = \sum m(1010,1011,1100,1101,1110,1111) \tag{3}$$

And can be written in literals as

$$F(ABCD) = \overline{A}\overline{B}C\overline{D} + \overline{A}B\overline{C}D + A\overline{B}\overline{C}D + A\overline{B}C\overline{D} + A\overline{B}CD + ABC\overline{D} + C_{out} \tag{4}$$

Karnaugh mapping is used to minimized the literals and hence reduce the number of gates that can be used to implement the circuit. Table 4 shows the mapping of the corresponding numbers.

TABLE 4, Karnaugh mapping

CD \ AB	00	01	11	10
00			1	
01			1	
11			1	1
10			1	1

TABLE 5:Reduction of Simplest boolean function for the Hexadecimal to decimal conbverter from K-map

<u>ABCD</u>	<u>ABCD</u>
1100	1111
1101	1110
1111	1011
<u>1110</u>	<u>1010</u>
<u>AB</u>	<u>AC</u>

Therefore the function reduced to

$$F(A,B,C,D) = AB + AC + C_{out} = A(B+C) + C_{out} \tag{5}$$

The logic function above can be implemented with logic gates as follows.

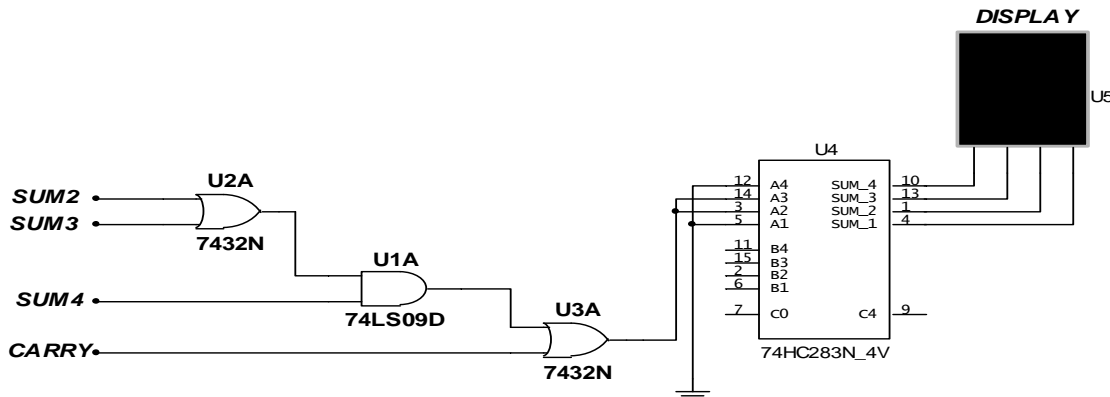


Figure 10: Hexadecimal code converter

The circuit in Figure10 has solved the problem of displaying in hexadecimal to some extent. But when the counting exceeds nineteen, another circuitry is needed which increment the tens display to a higher digit. This circuit is capable of detecting the numbers from twenty and above and adds binary six to recycle the unit display to remain within 0 to 9 and then increment the tens display from 1 to 2. A half adder is also needed to ensure that the tens display is incremented whenever there is a carry.The general output display circuitry is shown in Figure 10.

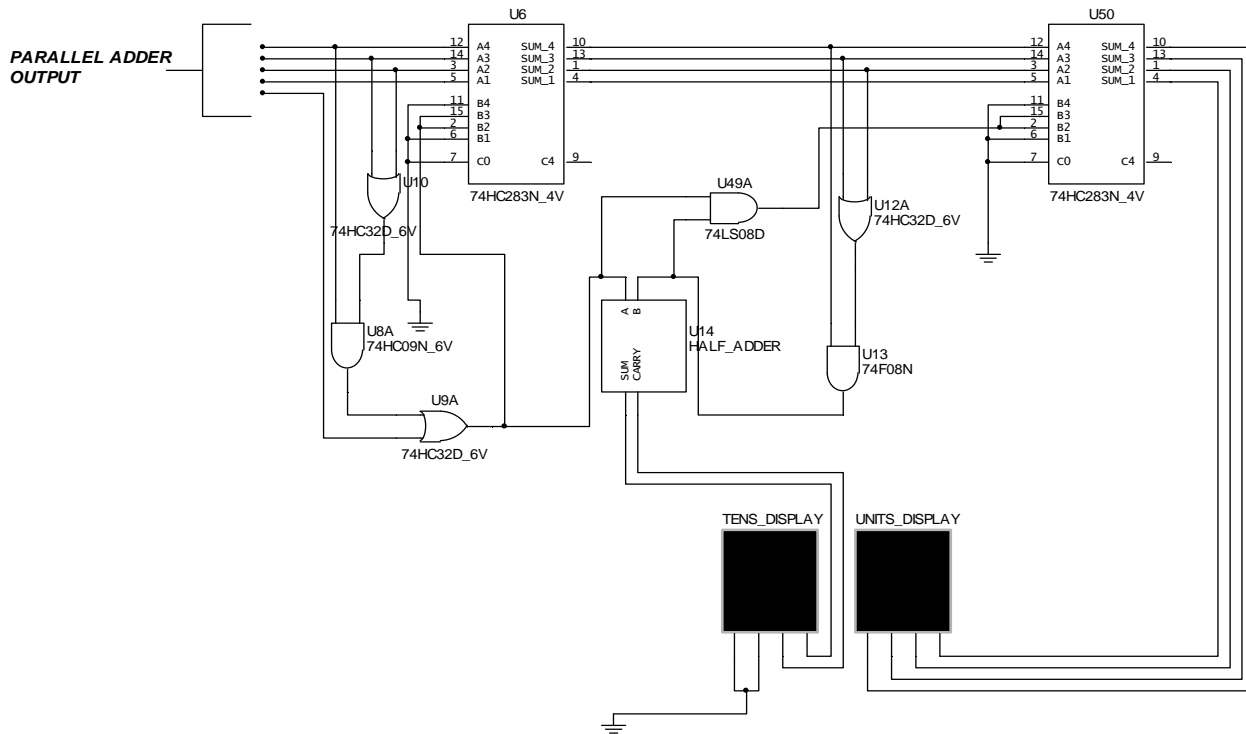


Figure 11. General output circuitry.

### 3.0 General Circuit

The general circuit of the voting machine as shown in figure 12 is design to accommodate all the previously discussed sections to have a constructive voting machine with a maximum number of 24 voters or parliament members depending on choose of selection of the user. From the figure it can be notice that whenever the Single Pole Double Throw (SPDT) is in the upward position it indicate that the vote is YES and whenever it is in the downward position it indicate that the vote selection is NO. Hence, if all the switches are in the upward position the number of voters or parliament members that vote for YES is 24 thus 24 will be displayed on the display, at the same time since the maximum number of switches available is 24 and has been exhausted for YES votes then the number of votes that vote for NO is zero (00) thus 00 will be displayed in the display for NO votes. Furthermore if any or some of the switches are now move downward for opinion change the number of voters that vote for YES will decrease with an increase in the number of voters that vote for NO. If for example eleven switches are move to the downward position the number of voters that vote for NO will be equal to the number of switches in the downward position and thus the same number will appear on the display in this case eleven (11) will be displayed. At the same time it will be notice that the number of those that vote for YES will decrease by the number of votes that votes for NO from the maximum number of selection switches; in this case since 11 vote for NO then thirteen (13) will be displayed for number of votes that votes for YES making a total of the complete 24 switches as shown in the figure. However the circuit can be upgraded to any number of voters as desired.

#### 3.1 Results Andanalysis

The circuit was designed successfully and is simulated on National Instrument multisim version 11.0. The simulation analysis shows that the circuit is working perfectly as expected. When tested the voting machine is capable of allowing voting between two political parties (with the name of each party tagged) while the result is displayed when the voting is in progress. Moreover, the circuit can be upgraded by either increasing the number of adders to accommodate large number of voters. The inputs are arbitrary selected for some number of votes for either “YES” or “NO” and the output is displayed. Table 6 shows the exact number of the inputs selected for both votes.

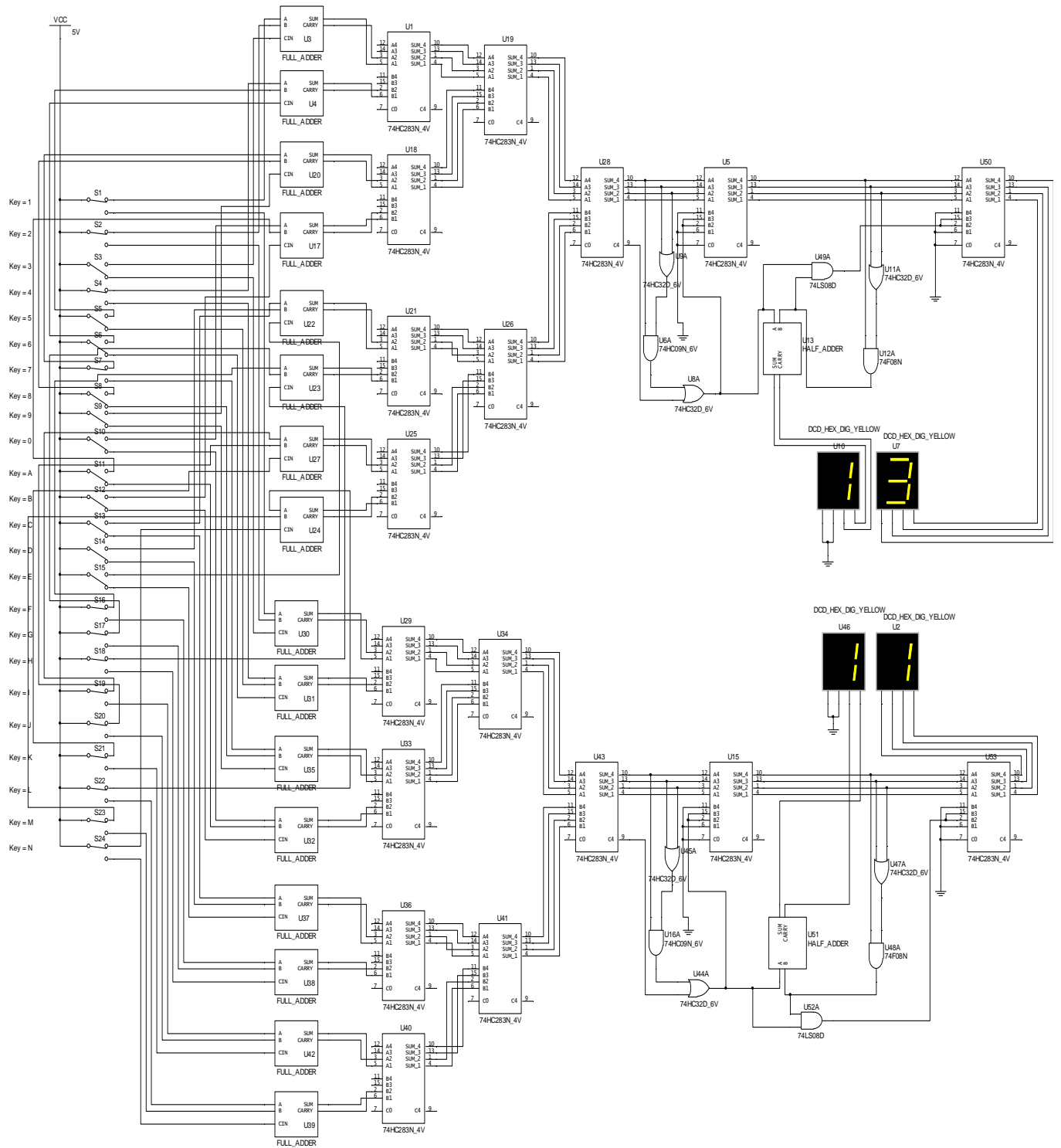


Figure 12: The general circuit diagram

**TABLE6: Result obtain from the display**

SWITCHES	POSITION “YES”	POSITION “NO”	POSITION NEUTRAL
SW 1	ON	OFF	
SW 2	ON	OFF	
SW 3	OFF	ON	
SW 4	OFF	ON	
SW 5	ON	OFF	
SW 6	OFF	OFF	ON
SW 7	ON	OFF	
SW 8	OFF	OFF	ON
SW 9	OFF	ON	
SW 10	ON	OFF	
SW 11	OFF	ON	
SW 12	ON	OFF	
SW 13	OFF	ON	
SW 14	OFF	ON	
SW 15	ON	OFF	
SW 16	ON	OFF	
SW 17	ON	OFF	
SW 18	OFF	ON	
SW 19	OFF	ON	
SW 20	OFF	ON	
SW 21	OFF	ON	
SW 22	ON	OFF	
SW 23	ON	OFF	
SW 24	ON	OFF	
<b>TOTALVOTES</b>	<b>12</b>	<b>10</b>	<b>2</b>

The switches are change as shown in the table and the result was recorded. The result shows that the displayed result tallies with the expected value.

### 3.2 Conclusion

The design and simulation of digital electronic voting machine was successfully carried out using full adders and parallel binary adders. The result obtain in the simulation analysis shows that the system work perfectly as desired were for a number of YES voters, 24 is displayed while 00 is displayed for NO voters and vice versa. Also the total number of YES and NO votes equal to the number of voters at any moment.

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