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# Design, Implementation and Simulation of Digital Clock Using Frequency Dividers and 555 Timer

***[1]Galadanci G.S.M., [2]Gana S. M. and [3]Abdullahi M.***
**[1,2]Physics Department,**
**Bayero University, Kano, P.M.B. 3011, Kano Nigeria.,**
**[3]Physics Department,**
**AuduBako Collage of Agriculture, Dambatta, Kano State**

***Abstract***

***In this work a digital clock was designed, implemented andsimulated. The design was carried-out using synchronous binary counters (74HC160D) and basic logic gates.The clock frequency to drive the clock was generated using a 555 timer. The counters were used as a divide-by-10 and a divide-by-6 for frequency division of the minutes and the second count. Also a divide-by-10 and a truncated sequence divide-by-10 were used for the hours count. The implemented digital clock circuit was simulated using windows based multisim( electronics workbench) software on personal computer (PC). The result of the simulation showed that the designed clock gives the approximate timing count, comparable with four different clocks purchased from the market. The designed clock functions as desired, where for every 60 second count one minute count was obtained and for every 60 minutes count 1 hour count was obtained. The clock recycled after every 12 hours count.***

## 1.0 Introduction

It is inevitable and imperative that the use of clock either analogue or digital is necessary to keep track of time for day to day activities.Acombination of devices designed to manipulate logical information or physical quantities that are represented in digital form called digital system are considered for the design of a digital clock. The main reason for the shift to this digital technology is because digital systems are generally easier to design, Information storage is easy, accuracy and precision are greater and more digital circuitry can be fabricated.This research provides basic information on how to design and implement a digital clock using combinational and sequential logic circuits[1]. These tools will be used to design the different parts of the clock and then implemented to create a customized clock. The clock will provide and keep track of seconds, minutes and hours information digitally. Synchronous binary counters are needed for this designand are operated using a 555 timer, Schmitt trigger or any other frequency generating device to generate a basic clock frequency signal in hertz[1,2].This signal is fed into the second section consisting of divide-by-60 counter (formed by cascading a divide-by-10 and a divide-by-6 counter) that counts from 00 to 59 and the recycles to 00 for count 60[2,3, 4]. The output of the second's section is fed into the minute's section which is similar to the second section where a divide-by-10 is truncated to 9 and its output is connected to divide-by-6 counter (formed by decoding divide-by-10 counter to count from 0 to 5 and recycle to 0)[2,3,4,5]. Finally, the output of the minutes counter is fed into the input of the hour section consisting of two divide-by-10synchronous 4-bit binary counters that counts from 01 to 12 and then recycles to 01, but additional circuitry are required for these operation[5]. These three sections are displayed using seven segment displays to show the second, minutes and hours. All these sections, are connected together to form the required design. The circuit can be implemented and tested using computer simulation software.

The main advantage of this research work is that the digital clock designed can be constructed using locallly abailable descrete digital components or can be implemented on any of the advanced programmable integrated circuit or microcontroller.

### 1.1 Binary Counter

A binary Counter is a digital circuitthat counts in binary. In digital system likecomputers, it is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal. It may also be considered as a type of memory that stores a binary number. Moreover, they can be used as instruments for detecting, counting, and indicating a sequence of events and can keep track of the number of input signal or pulses applied to it[1,5,6]. Its primary function is to produce a specified output pattern sequence. This

Corresponding author: ***Galadanci G.S.M.,*** E-mail: gsmgalad@gmail.com,, Tel.: +2348037260380

sequence might correspond to the number of occurrences of an event or it might be used to control various parts of a digital system. Binary Counters are made up of flip-flops and logic gate which like flip-flops can retain an output state after the input condition which brought about that state has been removed. However, while a flip-flop can occupy one of only two possible states, a counter can have more than two states. In the case of a counter, the value of a state is expressed as a multi-digit binary number, whose '1's and '0's are usually derived from the output of internal flip-flops that make up the counter[1,7,8]. The number of state a counter may have is only limited by the amount of electronic hardware that is available. The main types of flip-flops used are J-K flip-flop or T flip-flop. A Binary counter driven by a clock can be used to count the number of clock cyclesince clock pulse occur at known interval.The counter can be used as an instrument for measuring time and therefore period or frequency.

### 1.2 Asynchronous Binary Counter

Asynchronous counter is one in which the flip-flops (FF) within the counter do not change state at exactly the same time because they do not have a common clock pulse[1,5,9,10]. It is also called a ripple counter or a serial counter. Its clock input is applied only to the first flip-flop, also called the input flip-flop, and then the clock input to any subsequent flip-flop comes from the output of its immediately preceding flip-flop[11,12]. For instance, the output of the first flip-flop acts as the clock input to the second flip-flop, the output of the second flip-flop feeds the clock input of the third flip-flop and so on. In general, in an arrangement of n flip-flops, the clock input to the $n^{th}$ flip-flop comes from the output of the $(n-1)^{th}$ flip-flop for n>1[2,6,13].

### 1.3 Synchronous Binary Counter

Synchronous counteralso known as a parallel counteris actually a functional unit with a certain number of states, each representing a number which can be increased or decreased upon receiving an appropriate signal (e.g. a rising or falling edge pulse), and is usually used to count to, or count down to zero from, a specified number N[1,5,14,].Unlike ripple (asynchronous) counter, it contains flip-flops whose clock inputs are driven at the same time by a common clock line. This means that output transitions for each flip-flop will occur at the same time. Thus, the delay involved in this case is equal to the propagation delay of one flip-flop only, irrespective of the number of flip-flops used to construct the counter[4,13,14]. In other words, the delay is independent of the size of the counter. Since various flip-flops in a synchronous counter are clocked at the same time, additional logic circuitries are needed to ensure that the flip-flops toggle at the right time[10,15].

## 2.0 Design And Implementation

To design a digital clock that has an approximate time precision with any workable clock it is necessary to have knowledge on the basic ideas used for designing any digital system. For easier design, the main board of the digital clock is divided into five sub-circuits namely;

1. Power supply unit
2. Frequency generating circuit.
3. Second counter circuit.
4. Minute counter circuit.
5. Hours counter circuit.

These sections together form the digital clock. They can be implemented, tested and analyze quite easily if treated individually. Each of the sub-circuit is implemented by designing logic circuits that perform its duties. National instrument multisim software version 8.0 is used to simulate and test each section of the circuits mention earlier.

### 2.1 Power Supply Unit

The correct voltage supply is of utmost importance for the proper functioning of the digital clock system. For a perfect operation, it is necessary to provide a stable power supply: a RESET when it is turned OFF and SET when it is turned ON. According to technical specification, the 74XX (High speed CMOS) used for this design is between 2.5 V to 5 V for all components [6]. The simplest solution to the source of power supply is using the voltage stabilizer LM7805, which gives a stable voltage of +5 V from its output [5]. All safety precautions are properly observed. Moreover, in order to have stable 5 V at the output (pin3) of the LM7805, input voltage on pin1 should be between 7 V through 24 V. Also a 5 V DC battery can be used for this application. Fig.1 gives the circuit diagram of the power supply unit.

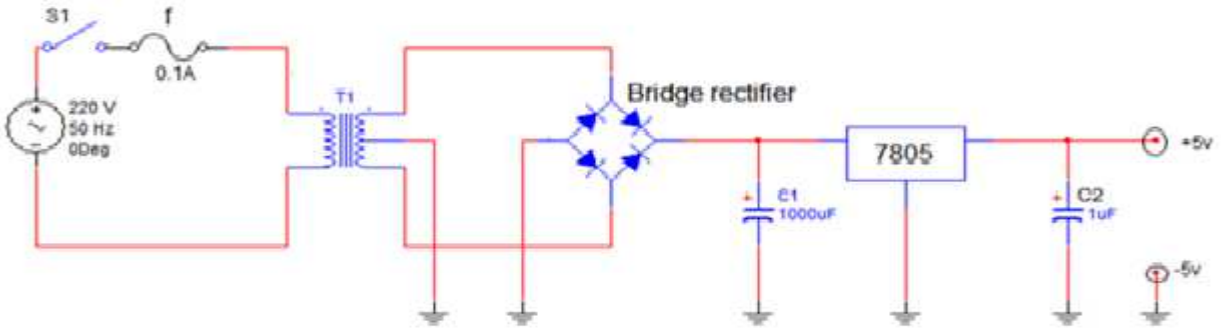


**Figure 1. Power Supply Unit**

2.2 FREQUENCY GENERATING CIRCUIT

The 555 timer connected to operate in an astable mode of operation can be used to generated a square wave in order to set/drive a digital clock operating with a frequency in hertz (HZ) or PPS (pulse per second). In order to achieve that, the resistors $R_1$, $R_2$ and the capacitor $C_1$ are varied accordingly until the desired frequency is achieved. Furthermore, it should be note that the 0.01µf capacitor C2 connected to the control input is strictly for decoupling and has no effect on the operation. And in some case it can be left off. However for this design two different frequencies are used in order to have the minimum and maximum value of the variable resistor, also the capacitor is variable. Before calculating the frequency, it should be noted that by making $R_2$ large with respect to $R_1$, we can get an essentially symmetrical square-wave output. Usually the value of the resistor $R_1$=1 KΩ because this helps to give the output pulses a duty cycle close to 50%, that is, the HIGH and LOW times of the pulses are approximately equal.

2.2.1 Calculation of the Working Frequencies

For frequency (F) of 500Hz, we assumed value of capacitor (C) to be 50µF. Since the value of the resistor $R_1$=1 KΩ so as to achieve a duty cycle of 50%, then

$$\text{Duty cycle} = \frac{t_1}{T} \times 100\% \quad (1)$$

Where $t_1$ = charge time (output HIGH).

Also;

$$T = \frac{1}{f} = \frac{1}{500} = 2 \times 10^{-3}\text{s} \quad (2)$$

Thus;

$$50\% = \frac{t_1}{2 \times 10^{-3}\text{s}}\ 100\% \quad (3)$$

$t_1 = 0.5\ (2 \times 10^{-3}\text{s}) = 1 \times 10^{-3}\text{s}$

Therefore;

$$t_2 = T - t_1 \quad (4)$$

Thus; $t_2 = 2 \times 10^{-3} - 1 \times 10^{-3} = 1 \times 10^{-3}\text{s}$

But;

$$t_2 = 0.693\ R_2C$$

Substituting for $t_2$ and C gives

$$R_2 = \frac{1 \times 10^{-3}\text{s}}{0.693 \times 50 \times 10^{-6}} = 28.86 \approx 29\ \Omega$$

Hence; for 500HZ: $R_1$ = 1kΩ, $R_2$ = 29Ω, C = 50µfandT = $2 \times 10^{-3}$s

Similarly,for frequency (f) of 800Hz, let's assumed value of capacitor (C) to be 50µF

Now; since the value of the resistor $R_1$=1kΩ so as to achieve a duty cycle of 50%

Then;Duty cycle = $\frac{t_1}{T} \times 100\%$ Where $t_1$ = charge time (output HIGH)

Also;

$$T = \frac{1}{f} = \frac{1}{800} = 1.25 \times 10^{-3}\text{s} \quad (5)$$

Thus;

$$50\%\ \text{Duty cycle} = \frac{t_1}{1.25 \times 10^{-3}\text{s}}\ 100\% \quad (6)$$

$$t_1 = 0.5\ (1.25\ \times 10^{-3}s) = 6.25\ \times 10^{-4}s$$

Therefore;

$$t_2 = T - t_1$$

$$t_2 = 2\ \times 10^{-3} - 6.25\ \times 10^{-4} = 1.375\ \times 10^{-3}s$$

Since; $t_2 = 0.693\ R_2C$

Substituting for $t_2$ and C

$R_2 = \frac{1.375 \times 10^{-3}s}{0.693 \times 50 \times 10^{-6}} = 9.92^{-8}\Omega = 0.0992^{-6}\Omega \approx 0.01\mu\Omega$

Hence; for 800HZ: $R_1$ = 1kΩ,$R_2$ = 0.01μΩ,C = 50μf and T = 1.25 $\times 10^{-3}$s

The minimum and maximum value of the variable resistor R2 to be use is calculated to be between 29Ω and 0.01μΩ respectively. Hence, the Fig.2 gives the complete set up of the 555 timer for frequency between 500 Hz and 800 Hz.

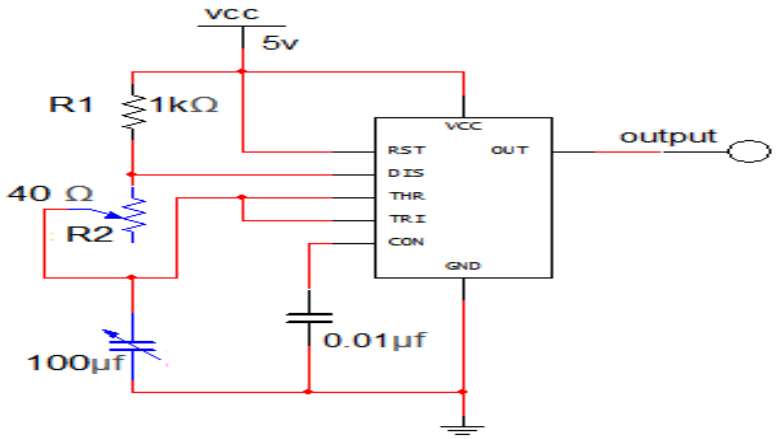


Figure 2: 555 Timer generating frequency between 500- 800 Hz

2.2.2 Second Counter Circuit

The second counter circuit is implemented and produced by divide-by-60 counter form by cascaded arrangements of two synchronous decade counters. The 1st counter is the divide-by-10 portion that counts from 0 to 9 and then recycles to 0 and the 2nd counter is the divide-by-6 portion that counts from 0 to 5 and then recycles to 0. The ripple clock output (RCO) of the 1st counter is connected to the enable inputs (ENP and ENT) of 2nd counter this allows the 1st counter to advances through all of its states from 0 to 9, on the clock pulse that recycles it from 9 back to 0 also called Terminal Count (TC), it goes HIGH and hence activates the enable inputs (ENP and ENT) of 2nd counter to illuminates a 1 on its display. The total count is now 10 (the 1st counter is in the zero state and the 2nd counter is in state 1). This process continues, for every terminal count of the 1st counter the 2nd counter advance to the next state in its sequence until the total count is 59 before all the two counters recycles to 00 for count 60 (1st Counter goes through ten complete cycles from 0 to 9 before counter 2 completes its first cycle). In general, the 2nd Counter is inhibited by the LOW on its Enable inputs until 1st counter reaches its last or terminal state and its terminal count output goes HIGH. In other words, for every ten cycles of counter 1, counter 2 goes through one cycle. Together these counters count from 00 to 59 and then recycle to 00. The terminal count, 59, is also decoded to enable the next Counter in the chain (minute circuit section). However, it should be noted that the divide-by-6 portion is formed with a decade counter with a truncated sequence achieved by using the decoder count 6 to asynchronously clear the counter. The figure 2.3 gives the second counter circuit diagram displaying 59 seconds.

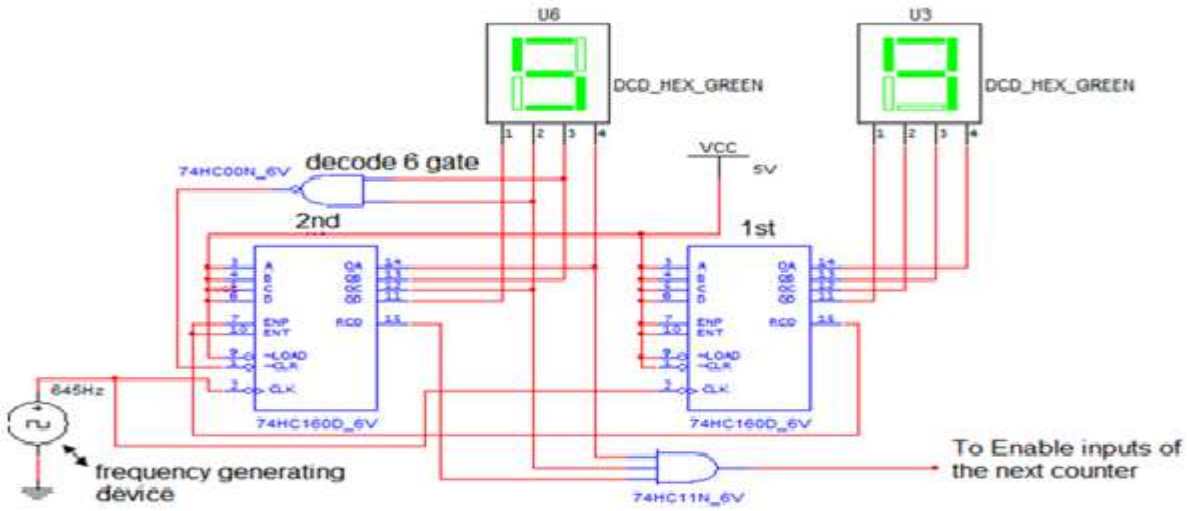


**Figure 3. Seconds/Minutes Section**

2.2.3 Minutes Counter

The minute circuit section is similar to the second circuit in its process of displaying its counts [Fig.3] however an additional circuitry is required to enable the divide-by-6 portion to have a perfect counting sequence [4,6,11,12].

2.2.4 Hours Counter Circuit

The hours counter is implemented and produce by cascaded arrangements of two synchronous decade (divide-by-10) counters as shown in [Figure 4]. The ripple clock output (RCO) of the 1st counter is connected to the enable inputs (ENP and ENT) of 2nd counter. The 1st counter advances through all of its states from zero to nine, on the clock pulse that recycles it from 9 back to 0 called Terminal Count (TC), it goes HIGH and hence activates the enable inputs (ENP and ENT) of 2nd counter to illuminates a decimal number, say 1 on its display. The total count is now 10 (the 1st counter is in the zero state and the 2nd counter is in state 1). Next, the total count advances to 11 and then to 12. In state 12 the $Q_B$ output of the 1st counter is HIGH and the 2nd counter is still HIGH, thus the decode-12 gate output connected to the LOAD input of the 1st counter is LOW since its inputs connected to but the $Q_A$ output of the 2nd counter and $Q_B$ output of the 1st counter are HIGH. This activates the LOAD input of the 1st counter. On the next clock pulse, the 1st counter is preset to state 1 by the data inputs, and the 2nd counter is preset to state 0 by a HIGH on the decode 1 gate which is connected to a NAND gate and its other input connected through an inverter to the LOAD gate so that whenever the LOAD is LOW the input of the NAND gate is HIGH. The HIGH's on but the input makes the output of the NAND gate connected to the CLEAR input of the 2nd counter LOW to clear the counter. As can be seen, this logic always causes the counter to recycle from twelve back to one rather than back to zero and the sequence continues.

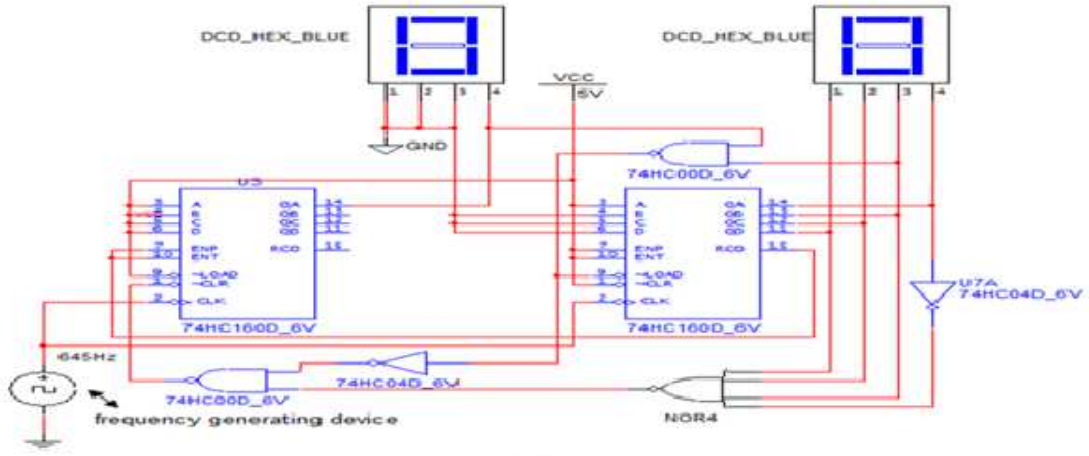


**Figure 4. Hours Section Circuit**

## 2.3 Design of the General Circuit Diagram of a Digital Clock

The general circuit of the digital clock is as shown in [Figure 5]. It is design to accommodate the five sections that constitute the digital clock in such a way that they can work synchronously with each other to have an appropriate and accurate timing system. These sections helps in the general operation of the digital clock. The main component that drives the clock from each of this section is the counters, which are marked and numbered from 1 to 6 accordingly for proper understanding. The 1st and 2nd counters are responsible for the second count; and the 3rd and 4th counters are responsible for the minutes count while the 5th and the 6th counter are responsible for the hours count. All of these sections are earlier discussed in the chapter. However, in order to connect all these three sections to work as whole, additional circuitries of combinational elements are required for succeeding counter in one section to Enable/clock its immediate proceeding section. In general Table 1 gives the name of component and series used for this design and the numbers marked on each of the so called component.

Table 1:List of Components used for implementation of the digital clock

| Name | Series | Number marked |
|---|---|---|
| 4-bit synchronous binary counter | 74HC160D | 1,2,3,4,5 and 6 |
| 2- inputs AND gate | 74HC11D | C1,C5,C9,C10,C16 and C17 |
| 2- inputs NAND gate | 74HC01D | C2,C3,C4 and C11 |
| 3- inputs AND gate | 74HC11D | C7 and C8 |
| 2- inputs OR gate | 74HC32D | C14 and C15 |
| 4- inputs NOR gate | | C6 |
| NOT(inverter) gate | 74HC04D | C12 and C13 |
| 7 segment LED display | DCD-hex | S1 to S6 |

The ripple clock output (RCO) of the 1st counter is connected to the enable inputs (ENP and ENT) of 2nd counter. The 1st counter advances through all of its states from 0 to 9, on the clock pulse that recycles it from 9 back to 0 also called Terminal Count (TC), the counter automatically goes HIGH and hence activates the enable inputs (ENP and ENT) of 2nd counter to advance to its next state, say 1. The total count is now 10 (the 1st counter is in the zero state and the 2nd counter is in state 1). This process continues, for every terminal count of the 1st counter the 2nd counter advance to the next state in its sequence until the total count is 59 before all the two counters recycles to 00 for count 60 second. However, for the second counter to Enable the minute counter a 3-input AND gate (C7) is used, where one of its input is connected to the Ripple Clocking Output (RCO) of the 1st counter and the remaining two are connected to $Q_A$ and $Q_B$ outputs of the 2nd counter to decode binary state 5 (0101) respectively, and its output is connected to an OR gate (C14) which allows the next counter (minutes counter) to advance to the required sequence of state when SET.

The output of this OR gate (C14) is the gate that is connected to the Enable input of the 3rd counter for minutes count, such that whenever the 2nd counter goes through all its state from 0 to 5 and the 1st counter advances through all of its states from 0 to 9, on the clock pulse that recycles but counters for count 60 all the 3 inputs of the AND gate are HIGH which automatically makes it output HIGH and hence activates the enable input of the minutes counter to illuminates a 1 on its display. This process continues, for every terminal count of the 1st and 2nd counter the 3rd counter responsible for minutes count advance through all of its states from zero to nine, on the clock pulse that recycles it from 9 back to 0 that is the Terminal Count (TC), it goes HIGH automatically and hence activates the enable inputs (ENP and ENT) of 4th counter to advance to its next state, say 1 Until its total count is 59 before all the two counters( 3rd and 4th) recycles to 00 for count 60 minutes repeating similar process as the second counter. Moreover, the OR gate (C14) allows the minutes counter to advance to next state in its sequence even before the terminal counts of the second section is reached by allowing signal from the AND gate (C16) to pass through one of its input whenever the output of the AND gate (C16) output is HIGH. This signal comes from the inputs of the AND gate (C14) which are connected to the clock pulse and switch 1 respectively such that whenever the switch is close the input to which it is connected goes HIGH and allows the clock pulse to pass to its output and then to the input of the OR gate (C14) to SET the minutes section to desired time. It should also be noted that an additional AND gate (C9) is connected to the Enable input of the 4th counter such that one of its input is connected to the output of AND gate (C7) and the other input to the Ripple Clock Output (RCO) of the 3rd counter for proper change in its sequence of state. This allows the 4th counter to advance through all its state whenever the output of the AND gate (C9) is HIGH every time its inputs (connected to C7 and RCO of the 3rd counter) are HIGH. The hours section used the same procedure as the minutes and second sections, the only difference is that the hours section is Enable by the minutes section through the output of the 3-inputs AND gate (C8) connected through an OR gate (C15) which allows the hours counter to advance to next state in its sequence even before the terminal count (TC) of the minute section is reached. The output of this OR gate (C15) is the gate connected to the enable input of the 5th counter for hours

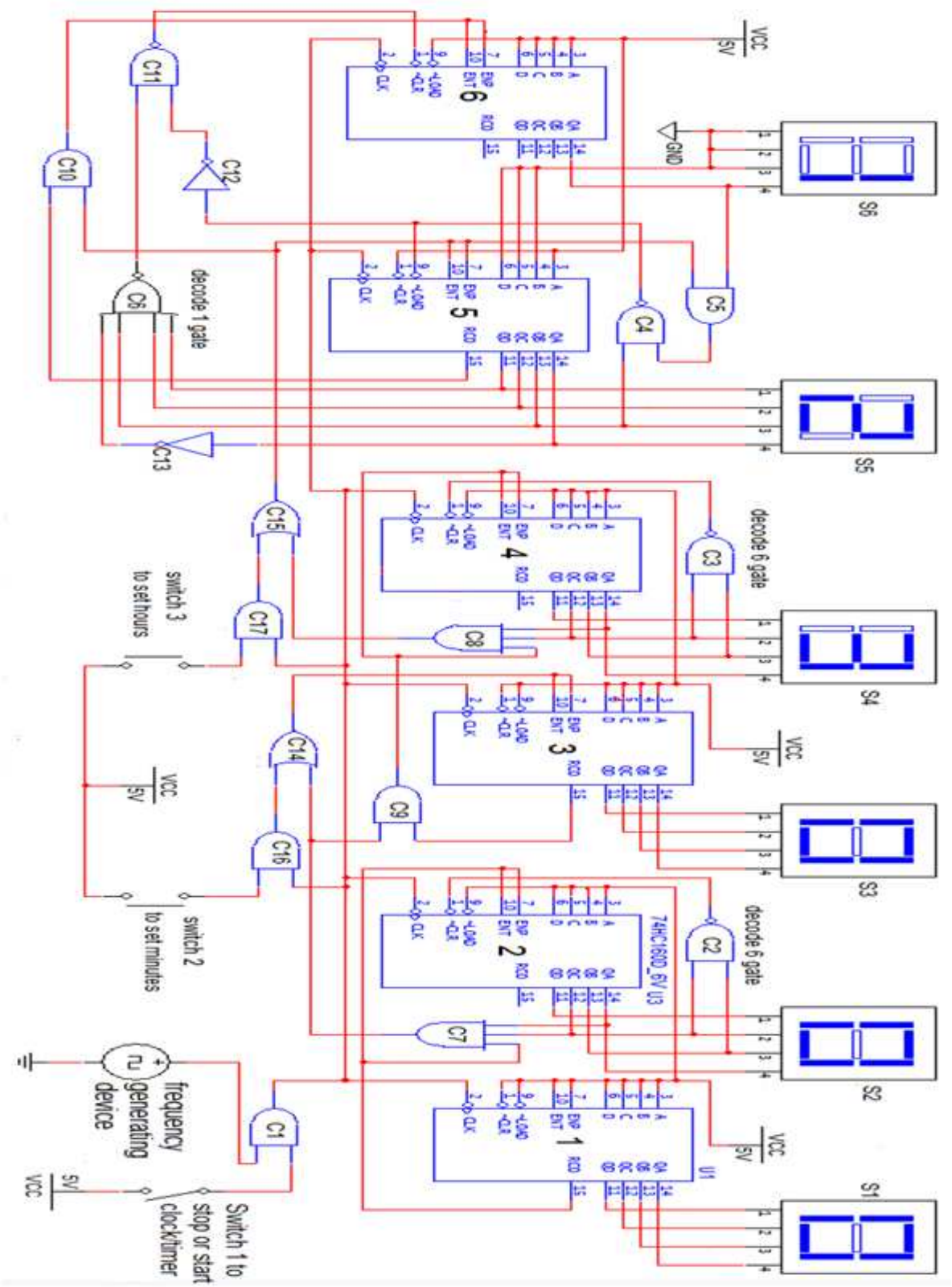


***Figure 5: General Circuit Diagram of the Digital Clock and timer***

count such that whenever any of its input is HIGH the counter advance one step in its sequence. Moreover, the OR gate (C15) allows the minutes counter to advance to next state in its sequence even before the terminal counts of the minute

section is reached by allowing signal from the AND gate (C17) to pass through one of its input whenever the output of the AND gate (C17) is HIGH. This signal comes from the inputs of the AND (C15) which are connected to the clock pulse and switch 2 respectively such that whenever the switch is close the input to which it is connected goes HIGH and allows the clock pulse to pass to its output and then to the input of the OR gate (15) to SET the hours section to desired time. Also for the hours section it should be noted that an additional AND gate (C5) is connected to one of the inputs of the NAND gate that LOAD count 1 so as to maintain the hours section at count 12 by keeping its output LOW until the Ripple clock input (RCO) of the $4^{th}$ counter to which it is connected is HIGH and also the other input connected to $Q_A$ output of the $6^{th}$ counter is HIGH.

### 2.3.1 Implementing The Designed Digital Clock As A Stopwatch

The AND gate (C1) can be used to start the digital clock by making its input HIGH and stop it by turning off the switch to keep its input LOW by allowing the clock pulse to pass through or to be inhibited respectively. This process of switching makes it possible for the digital clock to be used as a stop watch. Whenever the switch is close the stopwatch starts its count from 0 seconds to 12 hours maximum due to the clock pulse that the counters will receive and by turning off the switch the counts remain display on the LED displays until the switch is close again to RESET the count from 0 when a new clock pulse is receive.

## 3.0 Results And Disscusions

The analysis of combinational circuits starts with a given logic circuit diagram with a set of truth table or Boolean function, if the digital circuit is accompanied by a verbal explanation of its function, and the circuit is under investigation, it's necessary to interpret the operation of the circuit from the derived truth table for verification. The 4-bit synchronous binary counter is used to generate sequence of 16 different combinations of four digit binary code. But in the case of this design, the required sequence is from 0-9 and from count 10 to 16 are truncated hence brought about the used of 4-bit synchronous counter as a decade counter. However, in the process of designing a digital clock different sequence generating circuits are used for different sections. These sequences generating circuits are divided into three categories:

a) Two synchronous divide-by-10 counters that counts from 0 to 9 and then recycles to 0 (each one is use for second, minutes and hours count respectively).
b) Two divide-by-6 synchronous counters; decoded from divide-by-10 counters to count from 0 to 5 and then recycles to 0 (each one is use for second and minute count respectively).
c) Divide-by-10 synchronous counter, that count from 0 to 1 and then recycles to 0 for hours count.

This state generating circuit is what constitutes the design of the digital clock possible and helps in manipulating the counts to have an accurate precision. Table 2 below gives the inputs and the output displayed on the LED seven segment display of the divide-by-10 synchronous counter.

**Table2:**State generating sequence of a divide-by-10 counter

| DECIMALDIGITS | SEGMENTS INPUTS | | | | SEGMENTS OUTPUTS | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | D | C | B | A | A | B | C | D | E | F | G |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 2 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 3 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 4 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 5 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 6 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 7 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 8 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 9 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 10(recycles to 0) | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |

It should be noted that for the hours count, the counter advances through all of its states from 0 to 9, but on the clock pulse that recycles it from nine back to 0, it goes HIGH and hence activates the enable inputs (ENP and ENT) of $2^{nd}$ counter to illuminates a 1 on its display. The total count is now 10 (the $1^{st}$ counter is in the zero state and the $2^{nd}$ counter is in state 1). Next, the total count advances to 11 and then to 12. In state 12 On the next clock pulse, the $1^{st}$ counter is preset to state 1 by the data inputs, and the $2^{nd}$ counter is preset to state 0 by a HIGH on the decode 1 gate that is inverted to clear the counter. The state generating circuit sequence for the divide-by-6 synchronous counters input and its output on the segment display is indicated in Table3.

Table3: State generating sequence of a divide-by-6 counter

| DECIMAL DIGITS | INPUTS | | | | SEGMENTS OUTPUTS | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | D | C | B | A | A | B | C | D | E | f | G |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 2 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 3 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 4 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 5 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 6(recycles to 0) | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |

For the hours count, the state generating circuit sequence for the 2nd counter is as shown in Table4 below. However, it should be noted that its normal counting sequence is similar to that of Table 2 of the divide-by-10 counter, but because of the recycling effect that occurs in the counter when it's cleared to have the desired sequence (already discussed in the previews section) the counter only have two states 0 and 1.

**Table 4:** State generating circuit sequence for the 2nd counter

| DECIMAL DIGITS | INPUTS | | | | SEGMENTS OUTPUTS | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | D | C | B | A | A | B | C | D | E | F | G |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

To find the exact or approximate frequency required for a digital clock to have an accurate timing precision with every other clock, different stop watches (but of which are digital and analog) are used to compare the timing precision of the design clock in sixty seconds (60s) for different frequencies. The main aim of doing this analysis is to know the exact frequency that will enable the design digital clock to have an approximate or close timing precision with any clock in question. Table 5 below gives the comparison offrequencies used versus the time obtained for different stop clocks.

**Table5:** Frequency used versus the time obtained for different stop clocks

| Frequency used in hertz (Hz). | Time precision of three different digital stop watches in seconds(s). | | | Time precision of an analog stop watch in seconds(s). |
|---|---|---|---|---|
| | $T_1$ | $T_2$ | $T_3$ | $T_4$ |
| 500 | 68 | 69 | 68 | 68 |
| 550 | 65 | 65 | 65 | 66 |
| 600 | 61 | 62 | 63 | 62 |
| 650 | 60 | 60 | 59 | 60 |
| 700 | 56 | 56 | 56 | 56 |
| 750 | 53 | 54 | 53 | 53 |
| 800 | 52 | 51 | 51 | 52 |

Furthermore, average timing precision between the four different stop watches used in the experiment can also be used in analyzing the range of frequencies/frequency that are/is close or approximate to the required frequency for accurate timing sequence of the digital clock/ stop watch. The difference between Average time ($T_A$) and Time precision ($T_D$) of the design digital clock $T_A - T_D$ is what helps in giving an insight of the frequency range that can be more suitable. Table 6 gives the Average time ($T_A$) of the stop watches used and the difference between Average time ($T_A$) and Time precision ($T_D$) of the designed digital clock ( $T_A - T_D$ ). Note the positive sign on differences ( $T_A - T_D$) indicate that the design clock is moving at faster rate than the experimental rate to which it can be calibrated while the negative sign indicate that design clock is moving at slower rate than the experimental rate to which it can be calibrated.

**Table6:** Comparison of theaverage time ($T_A$) of the stop watches used and the difference between Average time ($T_A$) and Time precision ($T_D$) of the designed digital clock ( $T_A - T_D$ )

| Frequency Used in hertz (Hz). | Time precision of the designed digital clock ($T_D$) in seconds(s) | Average time ($T_A$) of the experimental stop watches In seconds(s). $(T_1 + T_2 + T_3 + T_4)/4$ | Difference between average time ($T_A$) and time precision of the designed digital clock ($T_D$).$T_A - T_D$ |
|---|---|---|---|
| 500 | 60 | 68.25 | 8.25 |
| 550 | 60 | 65.25 | 5.25 |
| 600 | 60 | 62 | 2 |
| 650 | 60 | 59.75 | -0.25 |
| 700 | 60 | 56 | -4 |
| 750 | 60 | 63.25 | -3.25 |
| 800 | 60 | 51.5 | -8.5 |

## Conclusion

In conclusion the design of the digital clock/stopwatch was successfully carried out using synchronous counter and basic logic gates. The designed system was implemented and simulated using electronics workbench. The result of the simulation shows that the system functions as desired, where for every 60 second there is one minute and for every 60 minutes there is 1 hour, until the clock reaches 12 hours before it cycle back to 1 hour.

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