

Investigation of the Effects of Cascading Multistage JFET Common Source Amplifier on Gain and Bandwidth

¹A.S. Gidado, ²G. Babaji, ³M.H. Ali, ⁴M. Bature and ⁵M. SA'ID

^{1,2,3} Department of Physics, Bayero University Kano

⁴Department of Physics, Federal University of Technology Minna

⁵Department of Physics, Gombe State University

Abstract

In this work, a high gain broadband amplifier incorporating cascaded common source amplifier configurations for gain enhancement and bandwidth shrinkage is proposed. We investigated and reported the characteristics of N-channel BF245A JFET. We recorded its drain characteristics up to a drain voltage of 30V, and its mutual characteristics over a gate voltage of 0 to -1.5V. A chain of four stage common source amplifier was used to study the effects of cascading on gain and bandwidth of the amplifier. Results from simulations revealed that for a single-stage, the gain was found to be 24dB while the bandwidth was found to be 0.59GHz. The two-stage cascade has a gain of 34dB and a bandwidth of 0.37GHz. The three-stage connection recorded a gain of 46dB and a bandwidth of 0.32GHz and finally for a four-stage cascade connection, the gain was obtained as 54dB while the bandwidth was obtained as 0.29GHz. In general, it was observed that as the number of stages was increased, there was a corresponding increase in the gain at the expense of the bandwidth.

Keywords: Artificial Neural Network; Concrete; Washed gravel; Regression; Modelling

1.0 Introduction

The performance obtainable from a single stage amplifier is often insufficient for many applications. In most applications, a single-transistor amplifier will not be able to meet the combined specifications of a given amplification factor, input resistance and output resistance. Hence several stages may be combined to form a multistage amplifier. These stages are connected in cascade, that is, output of the first stage is connected to form input of the second stage, and so on. Cascading is done either to increase the overall small signal voltage gain or provide an overall voltage gain greater than unity, with a very low output resistance. High speed multistage amplifiers are widely used in optical communication systems as the main amplifier in a receiver [1, 2,3]. Multistage amplifier topologies often provides a remedy for circuits with low gain. To increase the gain of a single stage amplifier, up to three or four equivalent simple gain stages can be employed. In a gain boosted amplifier, since miller compensation is avoided, we do not rule out the possibility of bandwidth limitations exhibited by the cascading approach [4].

The primary function of an amplifier is to reproduce the applied signal and provide some level of amplification. Unipolar transistors can be used to achieve this function. JFET and MOSFET are examples of unipolar amplifying devices. The *common-source amplifier* is the most widely used FET circuit configuration. The input signal is applied to the gate-source and the output signal is taken from the drain-source. The source lead is common to both input and output. A common-source amplifier has a very good ratio between input and output impedance. Circuits of this type are extremely valuable as impedance-matching devices. Common-source amplifiers are used almost exclusively as voltage amplifiers. They respond well in radio frequency signal applications [5].

The common-source amplifier has infinite input resistance and appreciable voltage gain. Both properties are useful and this is the most used of the FET linear circuits. Because of their low noise, FETs are often used in low-level audio frequency applications, e.g. in microphone head amplifiers where the high input resistance makes such amplifiers particularly suitable for following capacitor and piezo-electric microphones [6].

In general, a field effect transistor (FET) amplifier will have greater bandwidth than equivalent BJT topologies. Since the input resistance for the FET is very large, modelled as infinity, the low frequency pole contributed by this resistance and C_{in} will occur at low frequency. In addition, the device capacitances associated with FETs are generally smaller than those for a BJT. This has the effect of raising the upper cut-off frequency of FET amplifier relative to an equivalent topology BJT amplifier [7].

Corresponding author: A. S. Gidado, E-mail: gidadoa4217@buk.edu.ng, Tel.: +2348028276213

Journal of the Nigerian Association of Mathematical Physics Volume 23 (March, 2013), 423 – 434

This work intends to study the effects of cascading multistage common source amplifier on gain and bandwidth.

CIRCUIT TOPOLOGY

The common-source amplifier has characteristics similar to those of the common-emitter amp. However, the common source amplifier has higher input resistance than that of the common-emitter amplifier. The circuit for the common source amplifier is shown in Figure 1 [8].

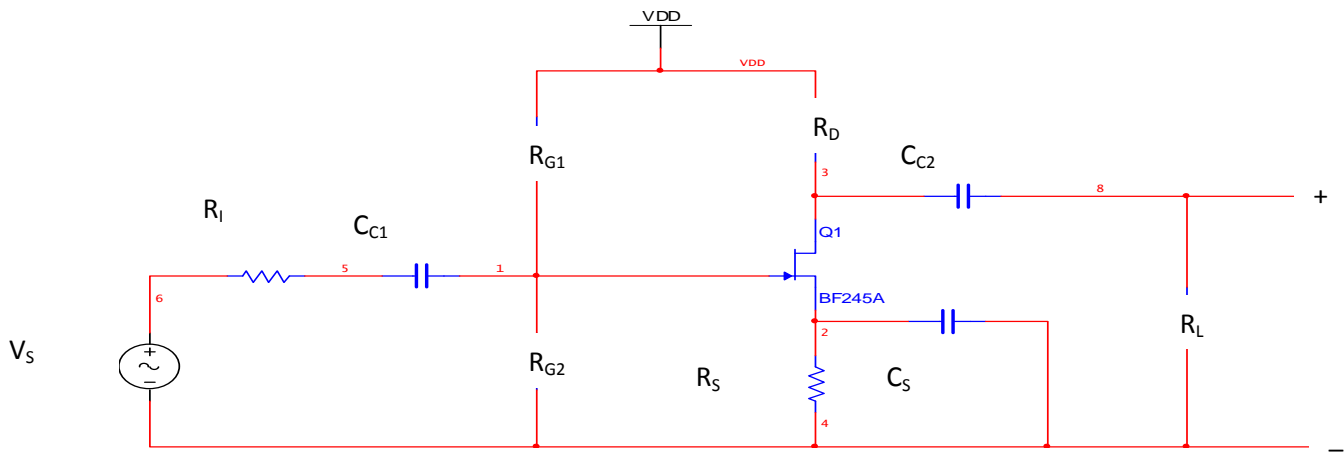


Figure 1 Single Stage Common Source Amplifier

The external capacitors C_{C1} , C_{C2} and C_S will influence the low frequency response. The internal capacitances of the FET will affect the high frequency response of the amplifier.

The midband gain, A_m , is obtained from the midband equivalent circuit of the common source amplifier. This is shown in Figure 2 . The equivalent circuit is obtained by short-circuiting all the external capacitors and open-circuiting all the internal capacitances of the FET.

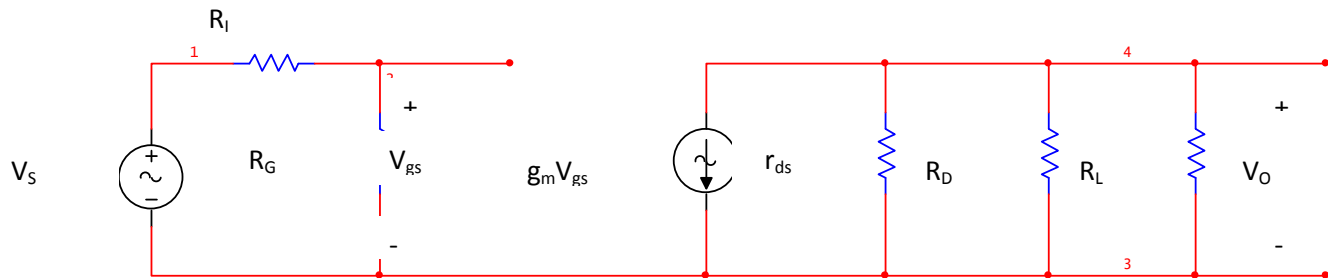


Figure 2 Midband Equivalent Circuit of Common Source Amplifier

Using the voltage division,

$$V_{gs} = \frac{R_g}{R_1 + R_g} V_s \tag{1}$$

From Ohm's law,

$$V_o = -g_m v_{gs} (r_{ds} \parallel R_D \parallel R_L) \tag{2}$$

Substituting Equation (1) into (2) , we obtain the midband gain as

$$A_m = \frac{V_o}{V_s} = -g_m \left(\frac{R_g}{R_g + R_1} \right) (r_{ds} \parallel R_D \parallel R_L) \tag{3}$$

At low frequencies, the small signal equivalent circuit of the common source amplifier is shown in Figure 3.0

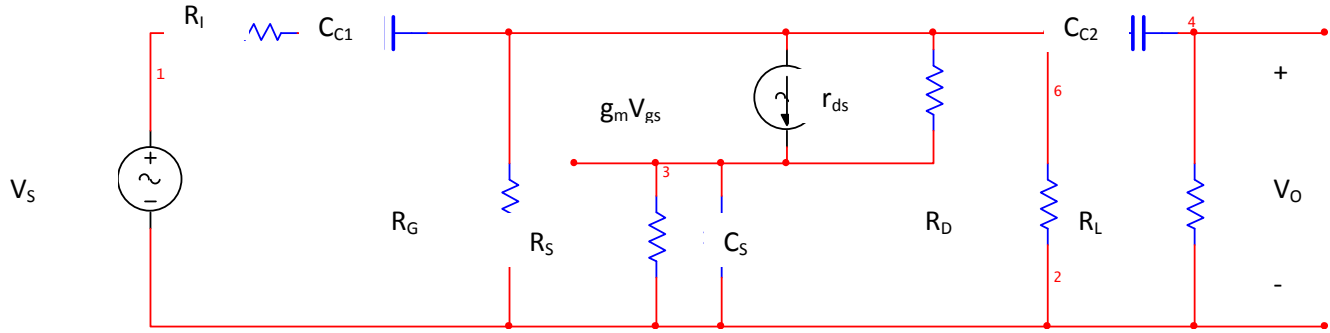


Figure 3 Equivalent Circuit for Obtaining the Poles at Low Frequencies of Common Source Amplifier

The low frequency poles due to C_{C1} and C_{C2} can be written as

$$\tau_1 = \frac{1}{\omega_{L1}} \cong C_{C1}(R_g + R_1) \quad (4)$$

$$\tau_2 = \frac{1}{\omega_{L2}} \cong C_{C2}(R_L + R_D \parallel r_{ds}) \quad (5)$$

Assuming r_d is very large, the pole due to the bypass capacitance C_S is given by

$$\tau_3 = \frac{1}{\omega_{L3}} \cong C_S \left(\frac{R_S}{1 + g_m R_S} \right) \quad (6)$$

and the zero of C_S is

$$\omega_z = \frac{1}{R_S C_S} \quad (7)$$

The 3-dB frequency at the low frequency can be approximated as

$$\omega_L \cong \sqrt{(\omega_{L1})^2 + (\omega_{L2})^2 + (\omega_{L3})^2} \quad (8)$$

For a single stage common source amplifier, the source bypass capacitor is usually the determining factor in establishing the low 3-dB frequency.

The high frequency equivalent circuit of common source amplifier is shown in Figure 4. In the figure, the internal capacitances of the FET, C_{gs} , C_{gd} and C_{ds} are shown. The external capacitors are short-circuited at high frequencies.

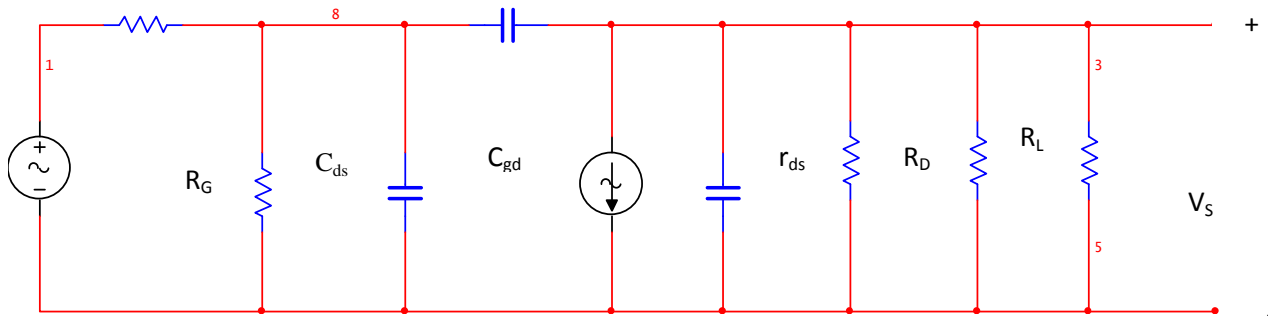


Figure 4 High Frequency Equivalent Circuit of Common Source Amplifier

Using the Miller theorem, Figure 4 can be simplified. This is shown in Figure 5.

The voltage gain at high frequencies is

$$A_V = \frac{V_o}{V_S} \cong - \left(\frac{R_G}{R_G + R_1} \right) \left(\frac{g_m R_L}{1 + s(R_G \parallel R_1) C_1 (1 + s R_L C_2)} \right) \quad (9)$$

where

$$C_1 = C_{gs} + C_{gd}(1 + g_m R_L) \quad (10)$$

and

$$C_2 = C_{ds} + C_{gd} \quad (11)$$

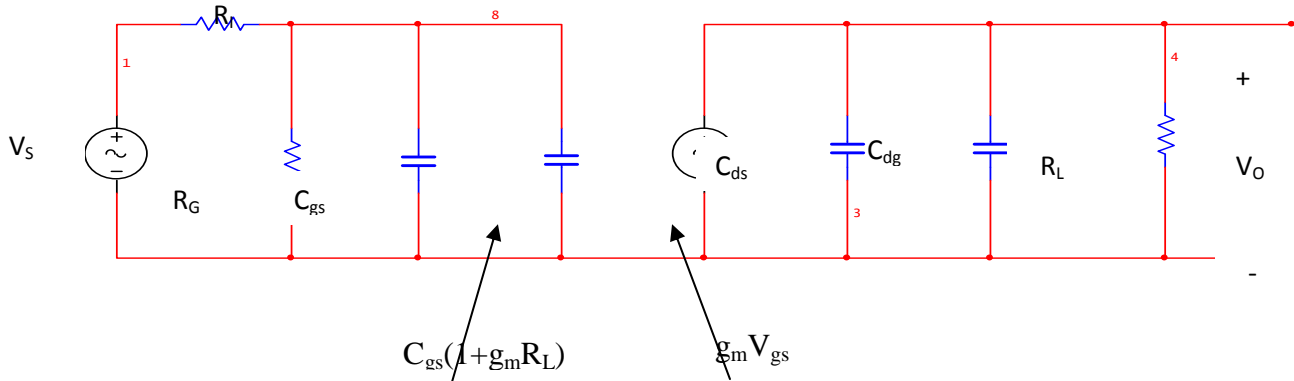


Figure 5 Simplified High Frequency Equivalent Circuit for common Source Amplifier

The high frequency poles are

$$w_{H1} = \frac{1}{c_1(R_G \parallel R_1)} \tag{12}$$

$$w_{H2} = \frac{1}{c_2(R_L \parallel R_D \parallel r_{ds})} \tag{13}$$

The approximate high frequency cut-off is

$$w_H = \frac{1}{\sqrt{\left(\frac{1}{w_{H1}}\right)^2 + \left(\frac{1}{w_{H2}}\right)^2}} \tag{14}$$

GAIN-BANDWIDTH CONSIDERATIONS

Consider a multistage amplifier with a DC gain A_A and a $-3dB$ bandwidth ω_A . Lets consider that the multistage amplifier is formed from a cascade of n identical stages, each with a single pole response [9, 10].

$$A_S(j\omega) = \frac{A_0}{1 + j\frac{\omega}{\omega_B}} \tag{15}$$

where A_0 is the DC gain and ω_B is the $-3dB$ bandwidth of each stage. Assuming that there is no interaction among the stages, then the overall transfer function of the multistage amplifier is

$$A_A(j\omega) = \left(\frac{A_0}{1 + j\frac{\omega}{\omega_B}}\right)^n, \text{ and} \tag{16}$$

$$A_A = A_0^n$$

The $-3dB$ bandwidth of the multistage amplifier ω_A is the frequency at which

$$|A_A(j\omega_A)| = \frac{A_A}{\sqrt{2}} = \frac{A_0^n}{\sqrt{2}} \tag{17}$$

Thus

$$\left[\frac{A_0}{\sqrt{1 + \left(\frac{\omega_A}{\omega_B}\right)^2}} \right]^n = \frac{A_0^n}{\sqrt{2}}, \tag{18}$$

$$1 + \left(\frac{\omega_A}{\omega_B}\right)^2 = 2^{\frac{1}{n}}$$

where

$$\omega_A = \omega_B \sqrt{2^{\frac{1}{n}} - 1} \tag{19}$$

The above relation shows that the bandwidth of the multistage amplifier ω_A will be less than the bandwidth of the individual stages ω_B . Increasing n , decreases ω_A , whereas enlarging the bandwidth of each stage, increases the overall bandwidth of multistage amplifier.

In general a cascade of n identical gain stages, each having a bandwidth ω_B , exhibits an overall bandwidth ω_A

$$\omega_A = \omega_B \sqrt[m]{2^{\frac{1}{n}} - 1}, \tag{20}$$

where m is equal to 2 for first-order stages and 4 for second order stages. The gain A_0 and bandwidth ω_B of each stage can be written in terms of the overall gain A_A and bandwidth ω_A as

$$A_0 = (A_A)^{\frac{1}{n}} \text{ and} \tag{21}$$

$$\omega_B = \frac{\omega_A}{m \sqrt{\frac{1}{2^n - 1}}} \tag{22}$$

An amplifier normally operates with signal frequencies between f_1 and f_2 . If the signal frequency drops below f_{c1} , the gain and thus the output signal level drops at 20dB/decade until the next critical frequency is reached. The same occurs when the signal frequency goes above f_2 . The range (band) of frequencies lying between f_1 and f_2 is defined as the bandwidth of the amplifier, only the dominant critical frequencies appear in the response curve because they determine the bandwidth.

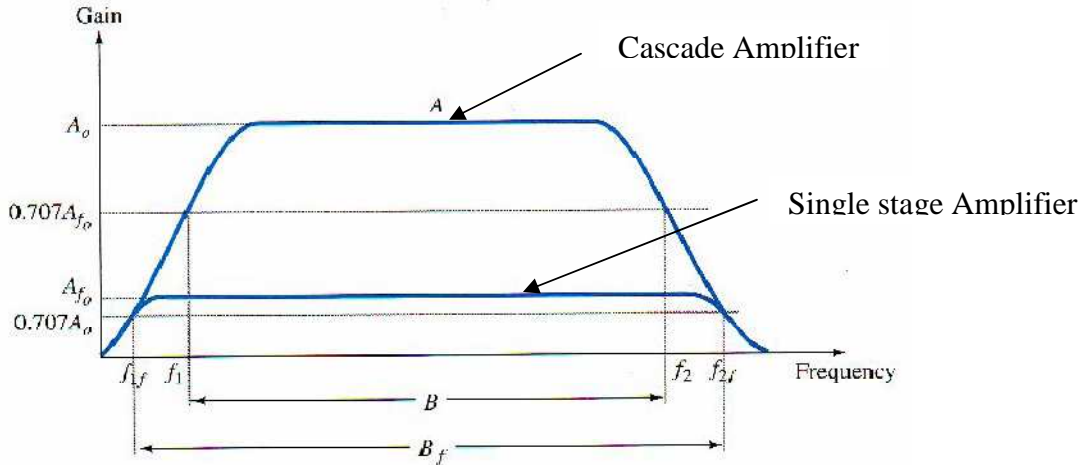


Figure 6 The frequency response

As the frequency response curve shows, the gain of an amplifier remains relatively constant across a band of frequencies. When the operating frequency starts to go outside this frequency range, the gain begins to drop off. Two frequencies of interest, f_1 and f_2 , are identified as the lower and upper cut-off frequencies [11].

The amplifier's bandwidth is expressed in units of hertz as [11]

$$BW = f_2 - f_1 \tag{23}$$

For the purposes of this discussion, the bandwidth is defined as the lowest frequency at which the voltage gain drops by $\sqrt{2}$ or 3dB. Accordingly this bandwidth is called the 3 - dB bandwidth [12].

Method and Materials

We applied computer simulation using MultiSim 8.0 to carry out this work. The drain and transfer characteristics data of JFET N-channel BF245A were obtained as described below.

For the transfer characteristics, the drain to source voltage (V_{DS}) was first adjusted to a suitable value of 10V and increased the gate to source voltage (V_{GS}) in small suitable steps of 0, -0.5, -1.0, -1.5, -2.0 and -2.5V. The corresponding value of drain current (I_D) was recorded for each step. A similar procedure was used for different values of $V_{GS} = 20V$ and 30V. The data obtained were used to plot a graph of V_{GS} along the horizontal axis and I_D along the vertical axis as shown in figure 6.0. For the drain characteristics, the gate to source voltage (V_{GS}) was first adjusted to zero volts and the drain to source voltage (V_{DS}) was then increased in small suitable steps of 2, 4, 6...30V. The corresponding value of I_D was recorded for each step. A similar procedure was used for different values of $V_{GS} = -0.5, -1.0, \text{ and } -1.5V$. The data obtained were used to plot a graph with V_{DS} along the horizontal axis and I_D along the vertical axis as shown in Figure 7.

From Figures 6 and 7, the values of $V_P, I_D, V_{DD}, V_{DS}, V_{GS}$ were obtained at quiescent points.

The drain current in the pinch off region depends upon the gate to source voltage and is given by the relation [13]

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2 \tag{24}$$

The pinch off region is the normal operating region of JFET when used as an amplifier.

The bias line satisfied the equations [14]

$$V_{GS} = -I_D R_S \tag{25}$$

$$V_{GG} = \frac{R_2 V_{DD}}{R_1 + R_2} \tag{26}$$

and

$$R_G = \frac{R_1 R_2}{R_1 + R_2} \tag{27}$$

Equation 26 only determines the ratio of the resistors R_1 and R_2 but in order to take advantage of the very high input impedance of the JFET as well as reducing the power dissipation within the circuit, we need to make these resistor values as high as possible with values in the order of 1 to $10M\Omega$ being common. [15]

The drain to source voltage of the output can be determined by applying Kirchhoff's law as follows [16]

$$V_{DS} + I_D R_D - V_{DD} = 0 \tag{28}$$

and

$$V_{DS} = V_{DD} - I_D R_D \tag{29}$$

To calculate the value of any coupling capacitor C_1 or bypass capacitor C_S , the standard formulas to be used are [17]

$$C_1 = \frac{1}{2\pi f R_{in}} \tag{30}$$

where $R_{in} = R_G$ and

$$C_S = \frac{1}{2\pi f R_0} \tag{31}$$

where $R_0 = R_D$

The equations above were used to obtain the relevant parameters needed to design the amplifier. A single stage common source amplifier was designed, and then cascaded to obtain a two-stage amplifier, three-stage amplifier and finally a four-stage amplifier. For a single stage amplifier, a sinusoidal input signal, $V_{in}, 40mV$ with a voltage of $10mV$ peak-to-peak value at frequency of $100Hz$ was applied. The output voltage, V_O , was observed and recorded. At fixed input voltage of $40mV$, the frequency was increased as: $1KHz, 10KHz, 100KHz, 1MHz, 10MHz, 100MHz$ and $1GHz$. In each case, a corresponding value of the output voltage was observed and recorded. The gain in decibel for each variation of frequency was calculated from [18]

$$A_V = 20 \log \left| \frac{V_{out}}{V_{in}} \right| \tag{32}$$

The data obtained were used to plot a graph of gain (dB) versus frequency (Hz) as shown in Figure 9. Origin 50 was used to plot the graph. In order to obtain the bandwidth, we used a screen reader from the menu of the origin to read values of lower cut-off frequency and upper cut-off frequency. The bandwidth is obtained as upper cut-off frequency minus the lower cut-off frequency. The same procedure was used for two, three and four stages amplifier. The input voltage ($40mV$) was constant at all frequency settings.

**RESULTS AND DISCUSSIONS
CHARACTERISTICS CURVES**

Figures 7 and 8 show the transfer and the drain characteristics of N-channel BF245A JFET. Values of V_P, I_D, V_{DS} , and V_{DD} were obtained from them. Table 1 is a summary of the various quantities used in the design and their values.

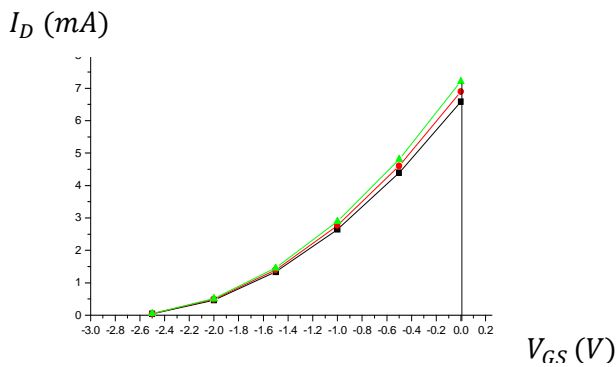


Figure 7 Transfer characteristics

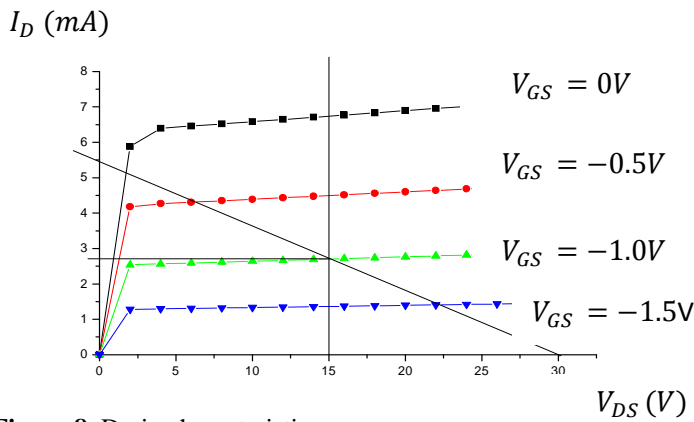


Figure 8 Drain characteristics

TABLE 1

S	QUANTITY	SYMBOL	VALUE
1	Drain current	I_D	$2.7mA$
2	Gate pinch-off voltage	V_p	$-2.5V$
3	Gate-to-source voltage	V_{GS}	$-1.0V$
4	Drain-to-source voltage	V_{DS}	$15V$
5	DC-supply voltage	V_{DD}	$30V$
6	Drain resistor	R_D	$5.6K\Omega$
7	Source resistor	R_S	370Ω
8	Resistor 1	R_1	$1M\Omega$
9	Resistor 2	R_2	$10M\Omega$
0	Coupling capacitors	$C_1=C_2$	$1.5nF$
1	Source capacitor	C_S	$270nF$

SINGLE STAGE COMMON SOURCE AMPLIFIER: The graph in Figure 9 shows the gain versus frequency for a single stage common source amplifier. The gain was obtained to be $24dB$ and the bandwidth was found to be $0.59GHz$. The gain is low at small frequencies, then rises as frequency increases, level off for further increases in frequency, and then begins to drop again at high frequencies. Response to a small signal - 100 Hz, and a large signal - 1GHz sine waves are shown in Figures 10 and 11 respectively.

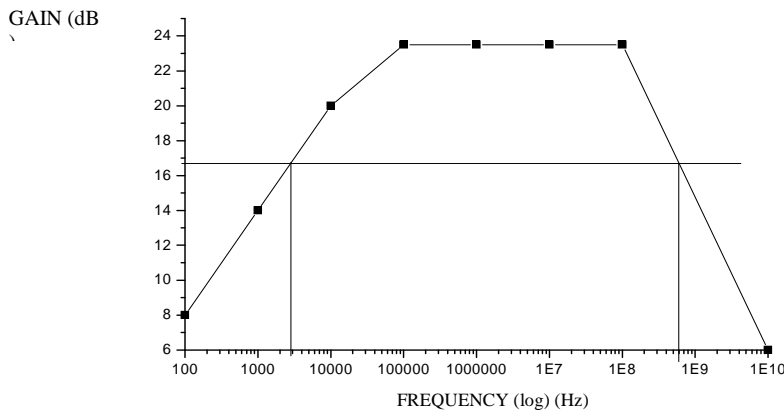


Figure 9 Graph of Gain(dB) versus Frequency (Hz) for Single-stage CS Amplifier

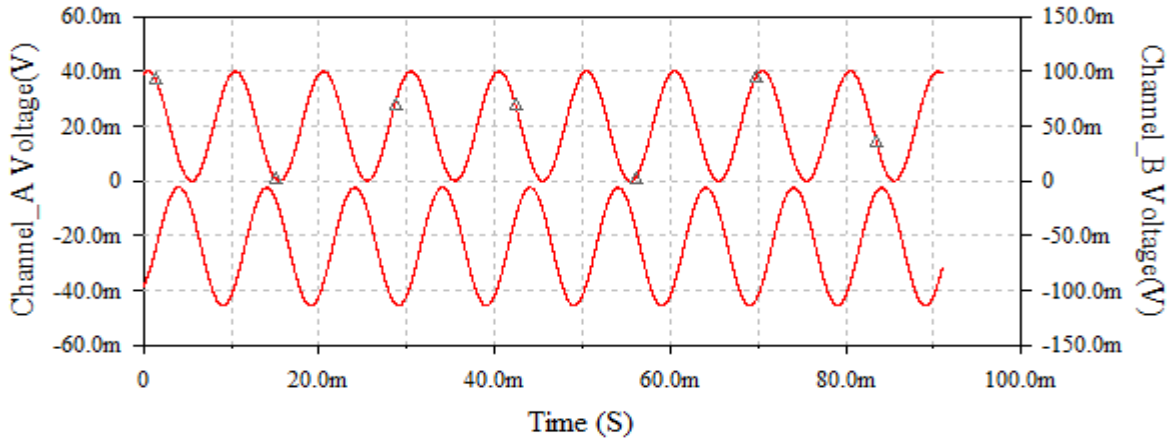


Figure 10 Single stage JFT common source amplifierResponse to a Small Signal - 100 Hz, sine wave

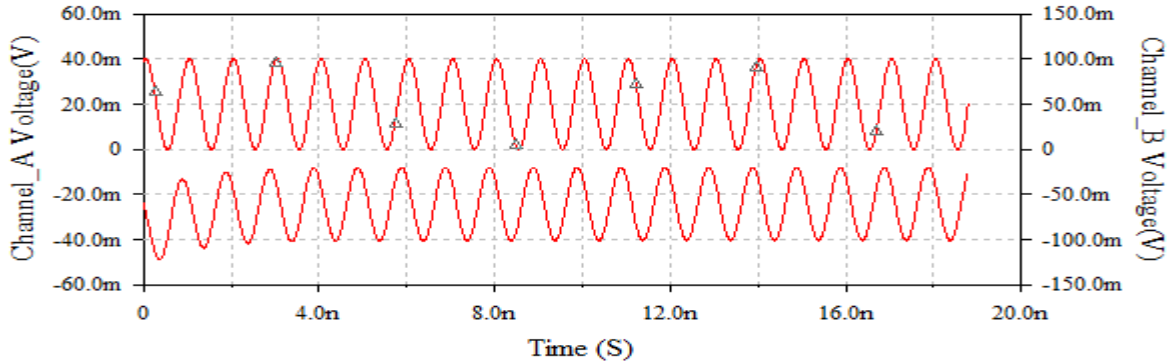


Figure 11 Single stage JFT common source amplifierResponse to a large Signal – 1GHz, sine wave

TWO-STAGE COMMON SOURCE AMPLIFIER: The graph in Figure 12 shows the gain versus frequency for a two-stage common source amplifier. The gain was obtained to be $34dB$ and the bandwidth was found to be $\approx 0.37GHz$. The gain is low at small frequencies, then rises as frequency increases, level off for further increases in frequency, and then begins to drop again at high frequencies. Response to a small signal - 100 Hz, and a large signal -1GHz sine waves are shown in Figures 13 and 14 respectively.

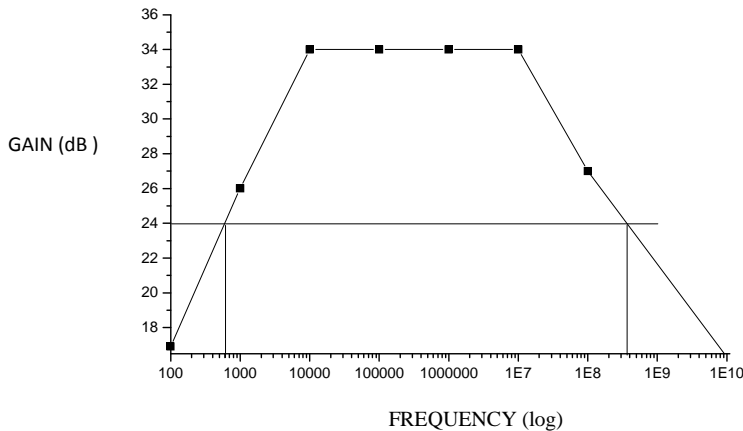


Figure 12 Graph of Gain(dB) versus Frequency (Hz) for Two-stage CS Amplifier

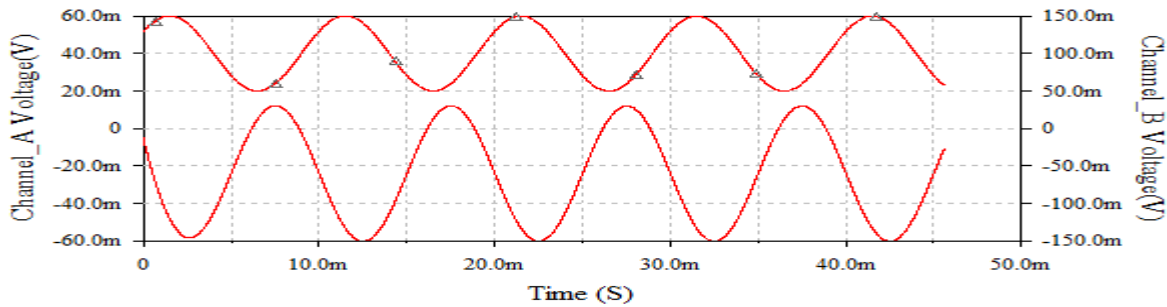


Figure 13 Two stage JFT common source amplifierResponse to a Small Signal - 100 Hz, sine wave

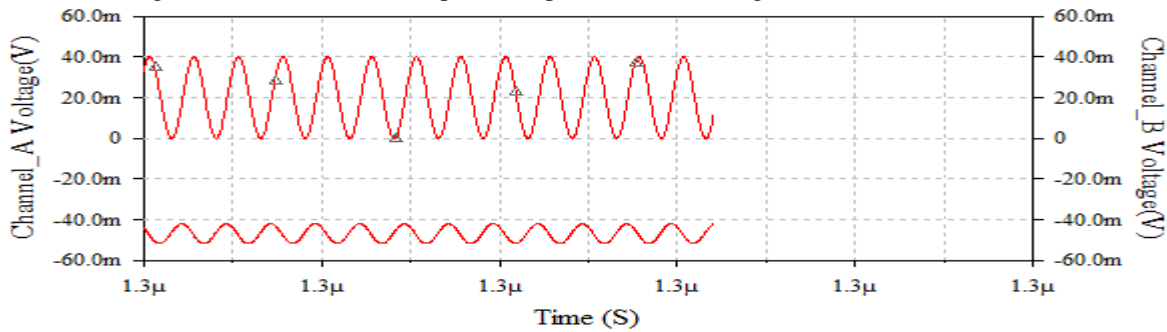


Figure 14 Two stage JFT common source amplifierResponse to a Large Signal - 1 GHz, sine wave

THREE-STAGE COMMON SOURCE AMPLIFIER: The graph in Figure 15 shows the gain versus frequency for a two-stage common source amplifier. The gain was obtained to be $46dB$ and the bandwidth was found to be $\approx 0.32GHz$. The gain is low at small frequencies, then rises as frequency increases, level off for further increases in frequency, and then begins to drop again at high frequencies. Response to a small signal - 100 Hz, and a large signal -1GHz sine waves are shown in Figures 16 and 17 respectively.

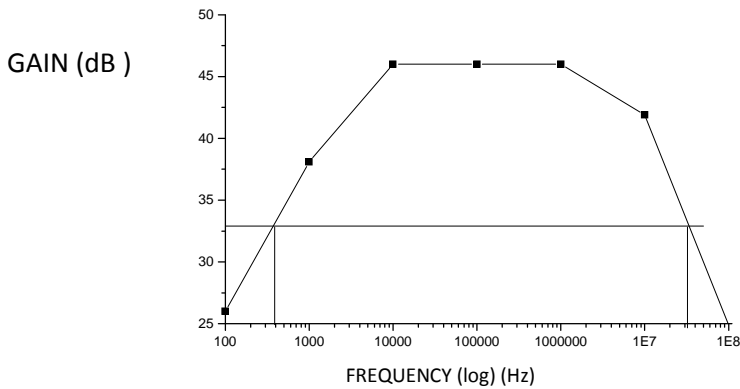


Figure 15 Graph of Gain(dB) versus Frequency (Hz) for Three-stage CS Amplifier

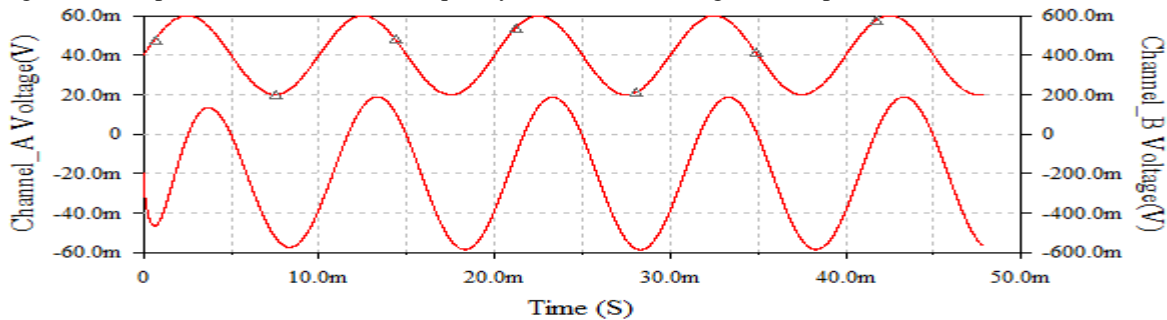


Figure 16 Three stage JFT common source amplifierResponse to a Large Signal – 100Hz, sine wave

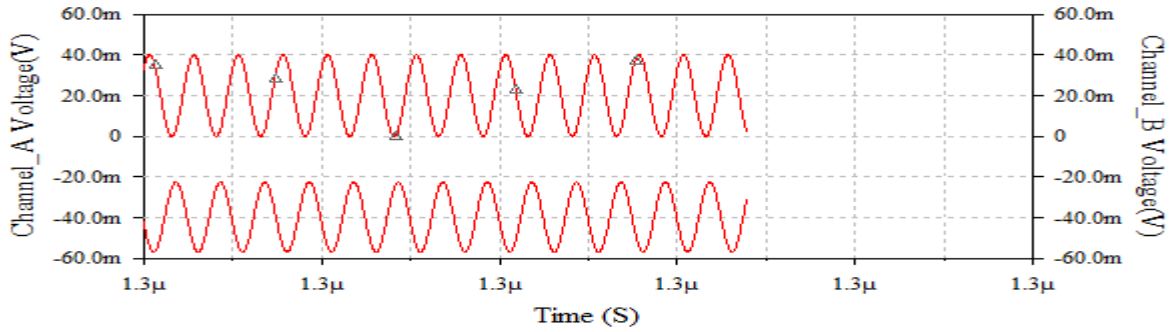


Figure 17 Three stage JFT common source amplifier Response to a Large Signal – 1GHz, sine wave

FOUR-STAGE COMMON SOURCE AMPLIFIER: The graph in Figure 18 shows the gain versus frequency for a two-stage common source amplifier. The gain was obtained to be $54dB$ and the bandwidth was found to be $\approx 0.29GHz$. The gain is low at small frequencies, then rises as frequency increases, level off for further increases in frequency, and then begins to drop again at high frequencies. Response to a small signal - 100 Hz, and a large signal -1GHz sine waves are shown in Figures 19 and 20 respectively.

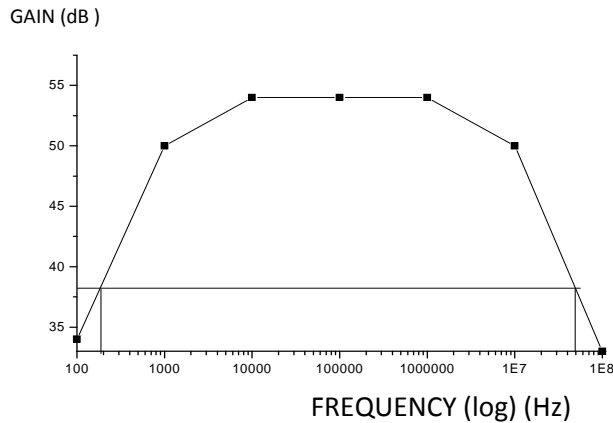


Figure 18 Graph of Gain(dB) versus Frequency (Hz) for Four-stage CS Amplifier

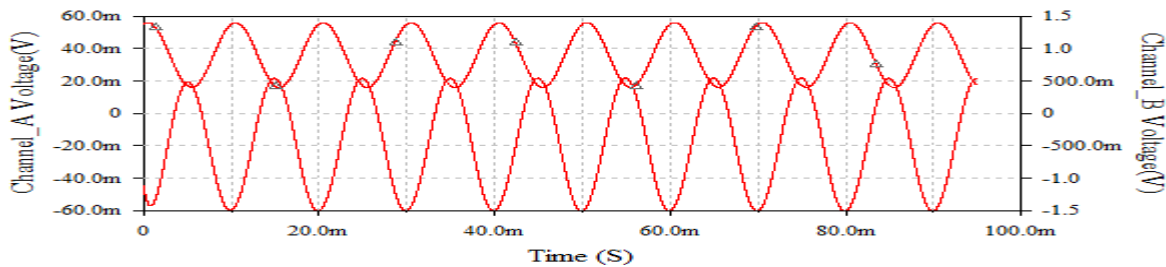


Figure 19 Four stage JFT common source amplifier Response to 100Hz, sine wave

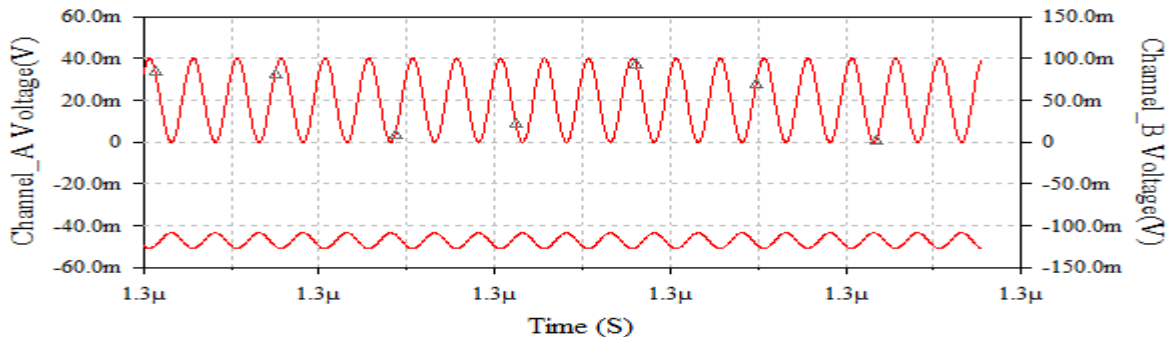


Figure 20 Four stage JFT common source amplifier Response to 100MHz, sine wave

TABLE 2 SUMMARY OF RESULTS

<i>Amplifier Mode</i>	<i>Single stage common source amplifier</i>	<i>Two stage cascaded common source amplifier</i>	<i>Three stage cascaded common source amplifier</i>	<i>Four stage cascaded common source amplifier</i>
<i>Gain (dB)</i>	24	34	46	54
<i>Lower cut-off Frequency (Hz)</i>	2826.16	203458.90	389.11	188.6
<i>Upper cut-off Frequency (Hz)</i>	592619622	371308083	323929252	287332283
<i>Bandwidth (Hz)</i>	592616796 ≈ 0.59GHz	371104624 ≈ 0.37GHz	323928863 ≈ 0.32GHz	287332094 ≈ 0.29GHz

Conclusion

In this work, a high gain broadband amplifier incorporating cascaded amplifier configurations for gain enhancement and bandwidth shrinkage is proposed. In a nutshell, by way of simulation using multiSIM8 Electronics Workbench and calculation using load line analysis and relevant equations, we were able to design a single stage common source amplifier, two-stage cascaded common source amplifier, three-stage cascaded common source amplifier and four-stage cascaded common source amplifier and studied their variation of output voltage with respect to frequency at constant input voltage of 40mV. We studied the effects of cascading on gain and bandwidth. We successfully showed that as the number of stages was increased, there was a corresponding increase in the gain at the expense of the bandwidth. This agreed with the theory that in a multistage amplifier, as the gain increases, the bandwidth decreases. Thus the decrease of bandwidth is proportional with the number of stages.

Reerences

[1] http://en.wikipedia.org/wiki/multistage_amplifier 14/05/2012
 [2] <http://www.mhhe.com/engcs/electrical/neamen01/ch06.pdf> 01/06/2012
 [3] B. S. Kwarik and M. S. Park, “Low-cost AlGaAs/GaAs HBT multi-gigabit limiting amplifier packaged with a new plastic air tight cavity encapsulation process,” *IEEE Trans. Components, Hybrids, and Manufacturing Technology*, vol.21, p. 310, Aug. 1998
 [4] B. Aishwarya , K. Bharani, S. Kommidi and K.J Naidu, “ Improvement of PSRR in Common Source Amplifiers” *IJAEST* Vol No. 6, Issue No. 1, p135 , 2011
 [5] Stephen W. F and Dale R.P., (2008), *Electricity and Electronics Fundamentals*, Fairmont Press Inc. 700 Indian Trail pp 155-156
 [6] Stan W. A and Mike R. J. , (2000), “ Principles of Transistor Circuits” , Clay ltd, St Ives Plc England, pp 84-85
 [7] http://www.eng.mu.edu/jacobyf/eece142/JFET_SSA_Design.pdf 23/09/2011.
 [8] Attia, J.O.,(1999) “Transistor Circuits.”*Electronics and Circuit Analysis using MATLAB*.Ed. John Okyere Attia Boca Raton: CRC Press LLC
 [9] S. Galal and B. Razavi, “10-Gb/s limiting amplifier and laser/modulator driver in 0.18-um CMOS technology,” *Solid-State Circuits, IEEE Journal of*, vol. 38, no. 12, p 214, 2003.
 [10] Centurelli, F.; Luzzi, R.; Olivieri, M.; Trifiletti, A., ‘A bootstrap technique for Wideband amplifiers," *IEEE Trans.Circuits and Syst-I*: vol. 49, p. 1479, 2002
 [11] http://Lec%5CBJT_Amp_freq_resp.pdf (05/04/2009)
 [12] B. Analui, and A. Hajimiri,. “Bandwidth Enhancement for Transimpedance Amplifiers” *IEEE Journal of Solid-State Circuits*, VOL. 39, NO. 8, p 1268, August 2004

- [13] Sedha, R.S, (2005) “ A textbook of Applied Electronics” S.Chand & Company ltd Ram Nagar, New Delhi pp 253-257
- [14] Millman J. and Halkias C., (2004) “ Integrated Electronics, Analog and Digital Circuits & Systems” Tata McGraw-Hill Publishing Company , New Delhi pp 337-338
- [15] (<http://www.scribd.com/doc/23913837/4/COMMON-SOURCE-AMPLIFIER> 07/03/2012
- [16] Boylested R.L and Kishore K.L,(2006) “ Electronic Devices and Circuit Theory” Dorling Kindersley(India) pvt ltd p389
- [17] <http://sound.westhost.com/valves/preamps.html> 09/02/2012
- [18] <http://www.engga.uwo.ca/people/adounavis/courses/ece241b/labs/lab6.pdf>27/09/2011