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DESIGN AND SIMULATION OF INTERLEAVED BUCK CONVERTER

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Abstract

In order to step down DC voltage effectively, it is sometimes important to use innovative buck converter technologies like the Interleaved Buck Converter (IBC). In this paper, a buck converter topology called the Interleaved Buck Converter is designed and simulated using LTSpice – a Simulation Program with Integrated Circuit Emphasis. The results were then compared to an ideal design and it was observed that the simulation results were very close to the theoretical design of the converter.

Keywords: LTSpice, Interleaved Buck Converter, Simulation, continuous conduction mode

1 Introduction

A buck converter is a step-down DC-DC converter. It uses a power semiconductor device as a switch to rapidly turn on and off the DC supply to the load. The switching action can be implemented by a Bipolar Junction Transistor (BJT), a Metal Oxide Semiconductor Field Effect Transistor (MOSFET), or an Insulated Gate Bipolar Transistor (IGBT) [1].

In order to satisfy the requirement of new electrical apparatus that work on high current and low voltages such as microprocessors, DC-DC converters that can supply regulated voltages from a constant power source are needed. The desired output parameters from the apparatus cannot be obtained with conventional Buck converters hence interleaved Buck converters are used to fulfil this requirement. The DC-DC Interleaved Buck converter is introduced to meet the increased demands such as low current ripple, high efficiency, faster dynamics, light weight and higher power density. The Interleaved Buck converter in this paper is designed to operate in the continuous conduction mode, this is done because the analysis is far easier than discontinuous conduction mode [2] however presents innovative numerical methods for analyzing Interleaved Buck converter in discontinuous conduction mode.

Section 2 provides the review of the method of interleaving buck converters and Section 3 presents the methodology employed in the research. The results and discussion are contained in Section 4 and in the end, the conclusion is presented in Section 5.

2 Interleaved Buck Converter

Interleaving also called multi-phasing, is a technique that is useful for reducing the size of filter components [3]. It is a way of connecting converters in parallel, interleaving means that N-identical converters are connected in parallel and the current through each switch is dispersed. When each converter provides the same current as the non-interleaved converter, the output current is N times higher. Therefore, the interleaved DC-DC converter is suitable to the low-voltage/high-current applications. Moreover, when the driving signals of N converters have $2\pi/N$ phase-shift one another, the output filter of the converter can be easily downsized [4]. With interleaving, power stage of a converter is divided into several and smaller power stages thereby reducing the size of each component [5]. The Interleaved buck converter is used in a lot of applications like LED Driver, this is as a result of the low current ripples and the reduced size of the reactive components [6].

The efficiency of the Interleaved Buck converter can be improved by changing the number of active phases in the network using digital controls, this was done by using a predictive algorithm to determine the duty of each phase, which will then result in equal current in the active phases, the circuit was simulated and it was discovered that the predictive current equalization scheme can equalize the phase currents in a single PWM period [7].

Structure of an Interleaved Buck Converter

The circuit diagram of an interleaved buck converter is shown in Fig. 2. The switches in the diagram are operated out of phase by 180^0, it is assumed that the circuit is operating in continuous conduction mode.

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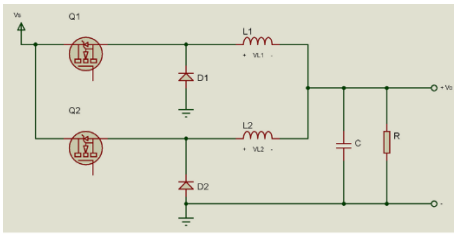

Fig. 2 Circuit diagram of a two-phase interleaved buck converter

The modes in which an Interleaved Buck converter operates is shown as follows.

Mode 1: In this mode switch Q1 is turned on by a gate pulse, while at the same time switch Q2 is off. Current flows through the switch Q1, inductor L1 and load, making current through L1 to increase as long as Q1 is turned on. During this time current in L2 decreases linearly. The equivalent circuit is as shown in Fig. 3. The variations of i_{L1} and i_{L2} during T_1 are given by Eq. (1) and Eq. (2) respectively,

$$\Delta i_{L1} = \frac{(V_S - V_O)}{L1} T_1 . \quad (1)$$

$$\Delta i_{L2} = \frac{(-V_O)}{L2} T_1 . \quad (2)$$

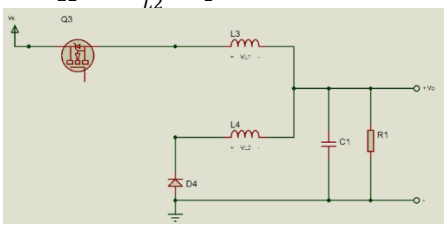

Fig. 3 Equivalent circuit of IBC in mode 1

Mode 2: In this mode both the switches in the circuit are OFF. Diodes D1 and D2 are the conducting devices. The equivalent circuit is shown in Fig. 4. The energies stored in L1 and L2 are released to the load through the forward biased diodes. So, the currents i_{L1} and i_{L2} are decreased linearly. Thus, the variations in i_{L1} and i_{L2} during T_2 are given by Eq. (4) and Eq. (5) respectively,

$$\Delta i_{L1} = \frac{(-V_O)}{L1} T_2 . \quad (4)$$

$$\Delta i_{L2} = \frac{(-V_O)}{L2} T_2 . \quad (5)$$

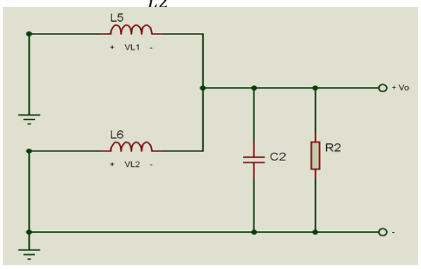

Fig. 4 Equivalent circuit of IBC in mode 2

Mode 3: During T_3, Q2 is turned on and Q1 turned off. The equivalent circuit is illustrated in Fig. 5. The turning on of Q2 charges the inductor L_2 and since Q1 is off inductor L_1 is discharged to the load. The variations in i_{L1} and i_{L2} during T_3 are given by Eq. (6) and Eq. (7) respectively,

$$\Delta i_{L1} = \frac{(-V_O)}{L1} T_3 . \quad (6)$$

$$\Delta i_{L1} = \frac{(V_S - V_O)}{L2} T_3 . \quad (7)$$

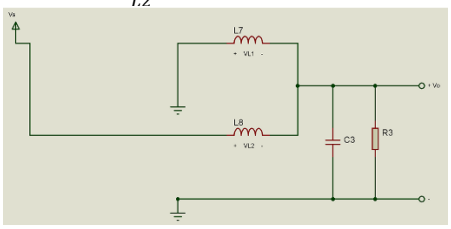

Fig. 5 Equivalent circuit of IBC in mode 3

A diagram of current waveforms through the inductor for the IBC is shown in Fig. 6.

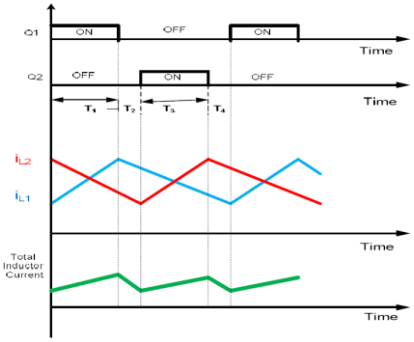

Fig. 6 Inductor current waveform

3 Experimental work

Design of the Interleaved Buck Converter

The Interleaved Buck Converter is designed to step down a 20VDC to 10VDC, the design is in continuous conduction ode and the output voltage ripple is 1%, the output power is 25%, switching frequency 31.33 kHz individual Inductor current ripple is considered as 5%. The calculations of the duty cycle, output current, output resistance and input current for the converter are shown in Eq. (8), Eq. (9), Eq. (10) and Eq. (11) respectively.

$$Duty\ ratio\ (D) = \frac{V_o}{V_s} = \frac{10}{20} = 0.5. \quad (8)$$

$$Output\ current = I_o = \frac{V_o}{V_s} = \frac{Po}{Vo} = 2.5A. \quad (9)$$

$$Output\ resistance = R_O = \frac{V_O}{I_O} = \frac{10}{2.5} = 4\Omega. \quad (10)$$

$$Input\ current = I_{IN} = I_O * D = 2.5 * 0.5 = 1.25\ A. \quad (11)$$

For two phase IBC, we can compute the inductance and capacitance values as shown in Eq. (12):

$$Inductor\ current\ I_{L1} = I_{L2} = \frac{V_O}{I_O} = \frac{2.5}{2} = 1.25A.$$

$$\Delta I_{L1} = \Delta I_{L2} = \frac{I_O/2}{100} * 5. \quad (12)$$

$$\Delta I_{L1} = \Delta I_{L2} = \frac{2.5/2}{100} * 5 = 0.0625.$$

Since ΔI_{L1}, ΔI_{L2} are out of phase and at the same value, they will cancel each other such that $\Delta I_{L1} + \Delta I_{L2} = 0$. Therefore, there is no need for the capacitor filter

$$L1 = L2 = \frac{(V_S - V_O)}{(\Delta I_{L1} \times n \times f) \times D}. \quad (13)$$

$$L1 = L2 = \frac{20-9}{5 \times 31.3k \times \frac{5 \times 2.77}{100}} = 47.99mH.$$

$$I_{min} = \frac{I_O}{2} - \frac{\Delta I_{L1}}{2} = \frac{2.5}{2} - \frac{0.125}{2} - = 1.187\ A$$

$$I_{max} = \frac{I_O}{2} + \frac{\Delta I_{L1}}{2} = \frac{2.5}{2} + \frac{0.125}{2} - = 1.31A$$

$$\Delta V_O = \frac{Vo}{100} = \frac{10}{100} = 0.1$$

Efficiency calculations

1. Losses in the switches due to drain-source resistance R_{NMOS}

$$P_{switch} = 2 \times R_{NMOS} \times \frac{I_O}{2} = 2 \times 0.077 \times (\frac{2.5}{2})^2 = 0.24W \quad (14)$$

2. Losses in the diode due to diode series resistance R_D

$$P_{diode} = R_D \times (I_O(1-D))^2 + V_F I_O(1-D) \quad (15)$$

$$P_{diode} = (0.3 \times (\frac{2.5}{2})^2 + (0.875 \times 1.25 \times .5)) \times 2 = 1.32W$$

3. Losses in the inductor due to internal series resistance RL

$$P_{inductor} = 2 \times R_L \times (I_O)^2 = 2 \times 0.6 \times (1.25)^2 = 1.875W \quad (16)$$

4. The input power is the sum of the output power and all the above losses.

$$P_{in} = P_{inductor} + P_{diode} + P_{switch} + P_o \quad (17)$$

$$P_{in} = 1.875 + 1.32 + .24 + 25 = 28.45W$$

5. Efficiency

$$= \frac{P_0}{P_{in}} \times 100 = (\frac{25}{28.45}) \times 100 = 87.87\% \quad (18)$$

4 Results and discussion

The Interleaved Buck Converter is simulated using LTSpice simulation software and the circuit diagram is shown Fig. 7. In the simulation, the switching losses are neglected.

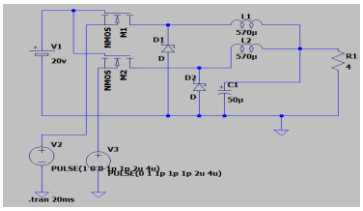

Fig. 7 LTspice circuit diagram for interleaved Buck converter

The input voltage signal to the buck converter is shown in Fig. 8 which is a unit input. The corresponding current is shown on the right vertical axis of the figure as well. Similarly, the output voltage is depicted in Fig. 9 as well as the output current in Fig. 10. Other important waveforms such as the voltages across the MOSFETs are shown in Fig. 11 and Fig. 12.

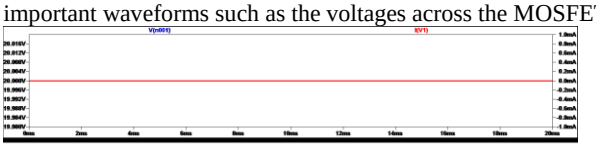

Fig. 8 Input Voltage

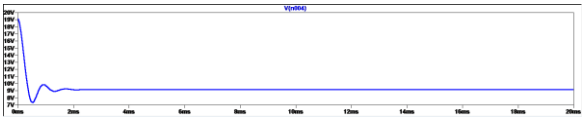

Fig. 9 Output voltage

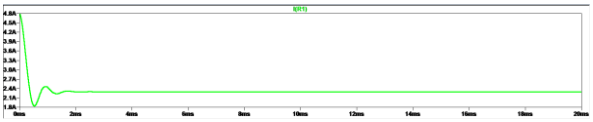

Fig. 10 Output current

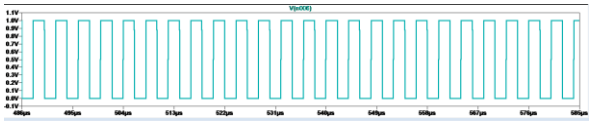

Fig. 11 Waveform of MOSFET 1

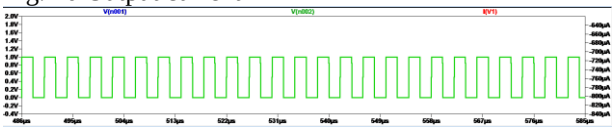

Fig. 12 Waveform of MOSFET 2

From the simulation results it can be seen that the values of the voltages and current gotten was very close to the theoretical design, hence it can be said that the circuit has been verified by simulation.

5 Conclusion

In this paper a two-phase Interleaved Buck Converter that is suitable for high current and low voltage applications was designed, this design was then simulated using LTSpice. In the simulation the transistors used were switched on and off by pulse width signals that were 180^{o} out of phase with each other. The efficiency of the Interleaved Buck converter and the results of the simulation are illustrated in this paper. A useful improvement to this work is the use of more phases in the interleaved Buck converter in order to improve the efficiency and output ripple of the converter.

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