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DESIGN OF AN OVERTEMPERATURE PROTECTION SYSTEM FOR AN LLC CONVERTER

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Abstract

Integrated circuits are composed of several transistors working together, at a particular temperature range. A change in the operating on-chip temperature affects the performance of the transistors, hence corrupting the processing efficiency of the entire IC. Internal Overtemperature protection, OTP is a safe way to deal with this problem. Internal OTP simply ensures the embedded transistor circuits only function within a convenient temperature range, such that the circuits are switched off as soon as the temperature increases beyond the safe-limit.

Keywords**:** OTP, IC, On-chip temperature, Embedded transistor

1 Nomenclature

DC/DC	Conversion from direct current to direct current
AC/DC	Conversion from alternating current to direct current
DC/AC	Conversion from direct current to alternating current
ZVS	Zero-voltage switching
LLC	Inductor-Inductor-Capacitor
PCB	Printed Circuited Board
PTC	Positive temperature coefficient
NTC	Negative temperature coefficient
RTD	Resistance Temperature Detector
Thermistor	A special resistor whose value varies with temperature
Thermocouple	Two different wires connected to measure temperature
diode-connected	Shorting the drain and source (or collector and base)
V_{BE}	Base-emitter voltage
$\propto_{V_{BE}}$	Temperature coefficient of the base-emitter junction
W/L	Ratio of width to length of the semiconductor channel
C_{OX}	Oxide capacitance
μ_n	Electron mobility
V_T	Threshold voltage
V_{GS}	Gate-source voltage
V_{GSF}	Compensated gate-source voltage
I_{DF}	Compensated drain current
I_D	Drain current
NMOS	n-channel MOSFET
PMOS	p-channel MOSFET

2 Introduction

Electrical appliances need electrical power to operate, hence the increasing demand for more efficient and high-power density DC/DC converters. This high density has become possible as the DC/DC converters are capable of operating at high frequencies [1]. Out of the several topologies of the DC/DC converters, the LLC resonant converter has proven to be reliable and capable of achieving a quality operation. It has special beneficial features such as ZVS (zero-voltage switching) capability for zero to full load range, impressively high efficiency at high input voltage, as well as a low voltage stress on the secondary rectifier stage. Since it doesn't require a filter inductor, the voltage stress on the rectifier diodes is minimized. From a design perspective, the LLC (inductor-inductor-capacitor) resonant converter is compact as the magnetic

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components can be integrated into one magnetic core. Another amazing thing is that even the leakage inductance of the transformer is utilized in the resonance conversion [1].

In reality, all power converters – AC/DC, DC/DC and DC/AC – consume power that is dissipated internally as heat. A lot of efforts have been put in place to remove the heat from the power dissipating components in order to keep the temperature of operation within the safe regions. The Arrhenius equation for reliability indicates that the failure rate of a power device will increase by 3 to 5 times for a 25℃ increase in temperature. The increasing demand for high power density converters which operate at higher junction temperatures, implies the need to handle these unfriendly operating conditions. The overall efficiency of the converter varies with the input voltage, output load and the operating. Function integration and high-switching frequencies and efficiencies have made it possible to minimize the physical volume of converters to a large extent. And the heat due to power dissipation have so far been removed by heat conduction techniques such as using heat sinks, PCB itself, potting material and the case of the component. But these techniques have an internal resistance against heat flow, hence reducing the efficiency in this method [2]. Conventional temperature sensors such as Thermistors (both PTC and NTC), RTDs, and thermocouples have also been employed to solve this problem of overtemperature operation. But the challenges have been either due to the problem of non-linearity in the voltage-temperature relationship or too small output voltage that needs extra amplification [3].

This paper introduces the diode-connected transistor configuration as an effective temperature sensor mechanism, especially as a key component in the internal overtemperature protection system in integrated circuits designed for power converters.

The diode-connected transistor as a temperature sensor

The BJT (bipolar junction transistor) is a very popular semiconductor device, and with the knowledge of the several benefits and versatility of semiconductor devices, it is no surprise that the transistor can perform excellently as a temperature sensor. The emitter-base voltage V_{BE} has a high temperature-dependence when connected in a diode fashion as shown in Fig. 1.

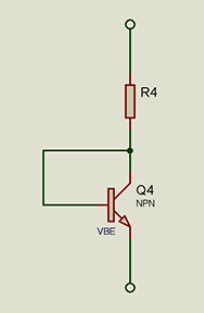

Fig. 1 A typical transistor diode-connected

It has been proven that there is a negative temperature dependence of the V_{BE} with temperature [4] and the mathematical equation to illustrate this temperature-dependence is given by Eq. (1);

$$V_{BE}(T) = V_{BE}(T_0) + \propto_{V_{BE}} (T - T_0). \quad (1)$$

Where $V_{BE}(T)$ is the base-emitter voltage at the new temperature, T.

$V_{BE}(T_0)$ is the base-emitter voltage at a reference temperature,

$\propto_{V_{BE}}$ is the temperature coefficient of the base-emitter junction

$T - T_0$ is the change in temperature.

In order to achieve a high sensitivity to temperature changes, the MOSFET is designed to have a low W/L [5].

Temperature characteristics of an NMOS transistor

The transconductance characteristics of an n-channel MOS transistor are described by Eq. (2);

$$I_D = 0.5\mu_n C_{ox} \left(\frac{W}{L}\right)(V_{GS} - V_T)^2. \quad (2)$$

Where C_{ox} is the oxide capacitance, the capacitance of the parallel-plate capacitor per unit gate area; W is the width of the channel; L is the length of the channel. μ_n is the mobility of the electrons at the surface of the channel, a physical parameter whose value depends on the fabrication process technology. V_{GS}, is the gate-source voltage, and V_T is the threshold voltage, the value of V_{GS} at which a sufficient number of mobile electrons accumulate in the channel region to form a conducting channel [6].

Both the mobility, μ_n and threshold voltage, V_T have a negative temperature dependence, such that when V_T is held constant and μ_n is allowed to change with temperature, the resulting plot is "flat" as higher temperatures are attained as shown in Figs. 2 and 3;

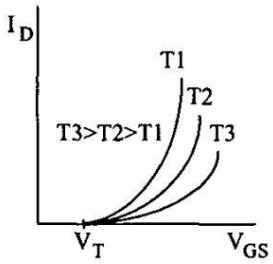

Fig. 2 V_T held constant

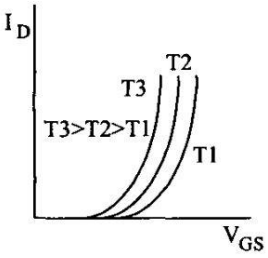

Fig. 3 μ_n held constant

But when μ_n is held constant and V_T is allowed to change with temperature, then the resulting plot will be closer to the coordinate origin at higher temperatures [6].

In the general case, when both and are allowed to change with temperature, the resulting plot forms a "bottleneck". The plot is as given in Figs. 4 and 5 [8] and the equations are given as;

$$V_T(T) = V_T(T_0) + \propto_{V_T} (T - T_0). \quad (3)$$

$$\mu_n(T) = \mu_n(T_0) \left(\frac{T}{T_0}\right)^{\alpha_\mu}. \quad (4)$$

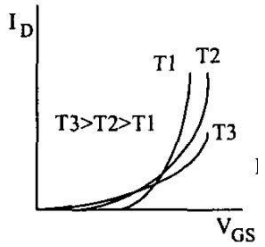

Fig. 4 V_T and μ_n allowed to vary

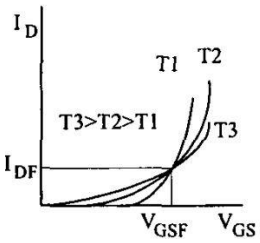

Fig. 5 Plot when $\alpha_\mu = \alpha_{\mu_0} = -2$

If the exponent $\alpha_\mu = \alpha_{\mu_0} = -2$ then one effect compensates another, and the characteristics intercept at the point (V_{GSF}, I_{DF}). Then, we have the relations for the parameters[8] of the point,

$$V_{GSF} = V_T(T_0) - \alpha_{V_T} T_0. \quad (5)$$

$$I_{DF} = 0.5\mu_n(T_0) C_{ox} {T_0}^2 \left(\frac{W}{L}\right) {\alpha_{V_T}}^2. \quad (6)$$

The Figs. 6 and 7 show the simulated transconductance characteristics of an NMOS transistor and a PMOS transistor, both designed in $0.18\mu m$ CMOS technology. It is evident from the plot that the NMOS transistor has a common intercept point while the PMOS transistor has no well-defined point, hence creating a "bottleneck". Hence biasing the NMOS to operate at this common intercept point by a current source, then its gate-source voltage will not temperature invariant. This is also called the Zero-Temperature Coefficient of the transistor [8].

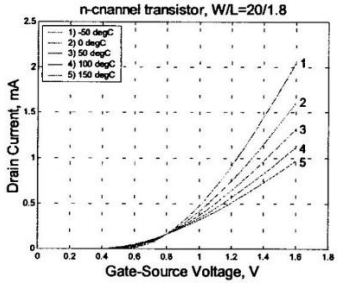

Fig. 6 Drain current relationship with gate voltage, NMOS

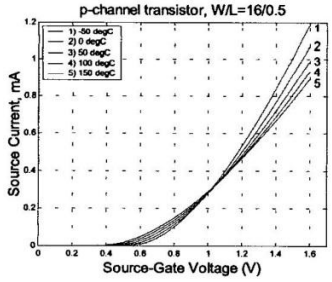

Fig. 7 Drain current relationship with gate voltage, PMOS

More on the gate-source voltage temperature dependence

When we substitute Eqs. (5) and (6) into Eq. (2), we get Eq. (7),

$$V_{GS} = V_{GSF} + \propto_{V_T} T \left\{1 - \sqrt{\frac{I_D/I_F}{(T/T_0)^{2+\propto_\mu}}}\right\}. \quad (7)$$

When $\propto_{\mu} = \propto_{\mu_0} = -2$, then Eq. (7) will get reduced to Eq. (8).

$$V_{GS} = V_{GSF} + \propto_{V_T} T\{1 - \sqrt{I_D/I_F}\}. \quad (8)$$

This result shows that in case of a constant drain current, the gate-source voltage is proportional to the temperature. The voltage either increases with temperature when $I_D > I_F$ or decreases with temperature when $I_D < I_F$. The simulation results obtained for the NMOS transistor with aspect ratio $\frac{W}{L} = \frac{20\mu m}{1.8\mu m}$, in solid lines (Fig. 8), using Eq. 8 with $V_{GSF} = 800mV$, and $I_{DF} = 162\mu A$, the dependencies are shown in star dots. In the case where $\propto_{\mu_0} \neq -2$, then from Eq. 7, the approximated quadratic dependence is given by;

$$V_{GS} \approx V_{GSF} + A_0 + A_1\left(\frac{\Delta T}{T_0}\right) + A_2\left(\frac{\Delta T}{T_0}\right)^2. \quad (9)$$

where $\Delta T = T - T_0$,

$A_0 = \propto_{V_T} T_0\left(1 - \sqrt{\frac{I_D}{I_{DF}}}\right)$, $A_1 = \propto_{V_T} T_0(1 + 0.5\alpha_{\mu_0}\sqrt{I_D/I_{DF}})$, $A_2 = 0.5\alpha_{V_T}T_0\sqrt{\frac{I_D}{I_{DF}}}(2 + \alpha_{\mu_0})$. As illustrated from Eq. 9, the closer α_{μ_0} is to -2, the smaller the non-linearity.

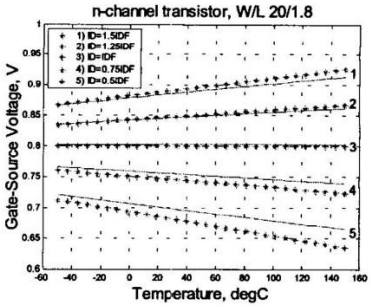

Fig. 8 Gate-voltage dependence with temperature

When the current source is now replaced with a resistor R_0, the current I_D has a variation given by,

$$\Delta I_D = -\frac{\Delta V_{GS}}{R_0}. \quad (10)$$

and $\Delta V_{GS} \approx A_1\left(\frac{\Delta T}{T}\right)$. Substituting $I_D + \Delta I_D$ instead of I_D, we get,

$$V_{GS} \approx V_{GSF} + A_0 + A_1'\left(\frac{\Delta T}{T}\right) + A_2\left(\frac{\Delta T}{T}\right)^2 . \quad (11)$$

$$A_1' = A_1[1 + (\propto_{V_T} T_0/R_0)(1/\sqrt{I_D I_{DP}})]. \quad (12)$$

A_2 will also vary if R_0 is linearly changing with temperature [8].

3 Experimental Work

Design and operation of the transistor overtemperature protection system

Fig. 9 shows the entire overtemperature protection system embedded inside an integrated circuit for a power converter. When the chip temperature exceeds the critical temperature, which is preset with OTP voltage, V_{OTP} in the LLC resonant converter, a triggering signal V_{OUT} is generated that causes the gate drive buffer circuit to put off the power switch. The main parts of the protection system are the bootstrapped comparator and the temperature sensor.

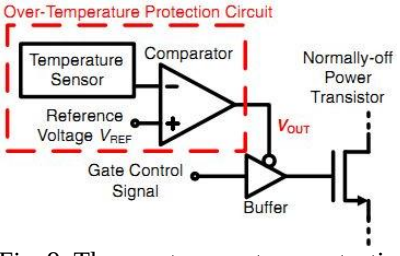

Fig. 9. The overtemperature protection system

The temperature sensor senses the chip temperature and produces a corresponding voltage, V_o . The V_o is fed into the bootstrapped comparator, and the comparator compares this V_o with the reference voltage, V_{REF}. Having temperatures above critical temperature translates to V_o being higher than V_{REF}, hence the comparator sends an ON signal. The signal is inverted through the buffer to control the power transistor. Hence this ON signal is inverted to an OFF which switches off the transistor.

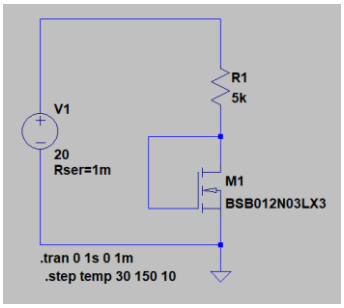

Fig. 10 Working of the temperature sensor circuit in LTSpice

The temperature sensor standalone circuit diagram is shown in Fig. 10. The NMOS transistor is connected in the diode-connected manner, and the transistor senses the temperature of the environment, through the p-n junction, thereby varying the gate-source voltage accordingly.

4 Results and Discussion

The simulation table given in Table 1 illustrates the variation of the V_{GS} with temperature for a an NMOS with part number BSB012N03LX3 that is shown in Fig.10.

Table 1 Gate-voltage against temperature

$\boldsymbol{T}$ (℃)	$\boldsymbol{V_{GS}}$ $\boldsymbol{(V)}$ $\boldsymbol{(@V_{DS} = 20V, R_D = 5k\Omega)}$
30	2.393
40	2.385
50	2.378
60	2.369
70	2.362
80	2.354
90	2.346
100	2.338
110	2.330
120	2.322
130	2.314
140	2.305
150	2.296

From the table, it is clear that as the on-chip temperature increases from the normal room temperature, the gate voltage decreases slightly. It is this change that is utilized to determine the temperature measurement. Fig. 11 shows a graph to establish the dependence of this particular NMOS transistor with temperature, without holding the drain current.

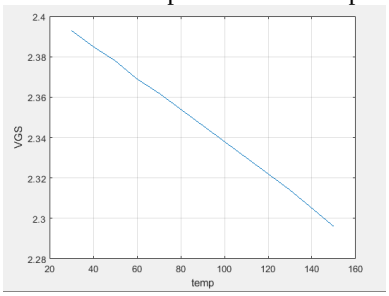

Fig. 11 Graph of gate voltage against temperature

Supposing the comparator reference voltage, V_{REF} is set to 2.305V, when the V_{GS} gets as low as 2.305V, indicating a temperature of 140℃, the comparator outputs a binary 0, since this is a common-mode condition. The binary 0 is passed through the voltage buffer and into the gate of the NMOS power transistor, hence switching it off. Typically, in the LLC resonant converter, this trigger action disables both the Half-bridge controller and the power factor controller. Then, when the temperature comes back to normal, the circuit undergoes a safe-restart.

5 Conclusion

With this work, it can be understood that overtemperature protection can be implemented inside an integrated circuit using transistors, using an NMOS as a case study. Having a transistor-based internal OTP is easier and offers a linear temperature dependence, as the conventional NTC system would pose a design challenge. NTCs could instead be employed as an external OTP.

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